

# Berry Discrete CFD Schematics Document

Clarksfield

Intel PCH

2010-07-15

REV : A00

*DY :None Installed*

*Madison:DIS Madison platform installed*

*M96:DIS M96 platform installed*

*VRAM\_128M:VRAM 128M\*16 installed*

*Colay :Manual modify BOM*

<Core Design>



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Title

**Cover Page**

Size  
A3

Document Number

**Berry**

Rev

**X00**

Date: Friday, July 23, 2010

Sheet 1 of 92

# DG15 MLK Block Diagram (Discrete only)

Project code : 91.4HH01.001  
PCB P/N : 48.4HH25.0SA  
PCB NO : 10215-SA

#OnMainBoard  
Madison LP; 1GB (64Mx16b\*8)  
VRAM Hynix 64M  
Wistronl P/N:72.51G63.C0U  
VRAM Samsung 64M  
Dell P/N:9TGTN\$AA  
Wistronl P/N:72.41164.H0U

Clock Generator  
SLG8SP585 7

AMD Graphic  
Madison-LP  
(Discrete only)  
80, 81, 82, 83, 84

VRAM  
1GB  
85, 86, 87, 88

DDR3  
800MHz

Intel CPU  
Clarksfield  
8, 9, 10, 11, 12, 13, 14

DDRIII 800/1066 Channel A

DDRIII Slot 0  
800/1066 18

DDRIII 800/1066 Channel B

DDRIII Slot 1  
800/1066 19

HDMI  
57

LCD  
54

CRT  
Left Side:  
USB x 2

CRT Board  
77

Bluetooth  
73

CAMERA  
54

Intel PCH  
HM57  
14 USB 2.0/1.1 ports  
ETHERNET (10/100/1000Mb)  
High Definition Audio  
SATA ports (6)  
PCI Express (8)  
LPC I/F  
ACPI 1.1  
PCI/PCI BRIDGE  
20, 21, 22, 23, 24, 25, 26, 27, 28

I/O Board  
Connector  
76

Mini-Card  
802.11a/b/g

10/100 NIC  
Realtek  
RTL8103T-VB

RJ45  
CONN

ESATA/USB  
Combo

Mini-Card  
WWAN

SIM

Right Side:  
USB x 1

CardReader  
Realtek  
RTS5159 78

SD/MMC+/MS/  
MS Pro/xD

Azalia CODEC  
IDT  
92HD79B1 30

HP1  
MIC IN

2CH SPEAKER

Flash ROM  
4MB  
62

LPC debug port  
70

HDD  
59

ODD  
59

KBC  
NUVOTON  
NPCE781BA0DX 37

Flash ROM  
256kB  
62

Touch  
PAD  
68

Int.  
KB  
68

Thermal  
Main:G7922  
Sec.EMC2102  
39

Fan  
58

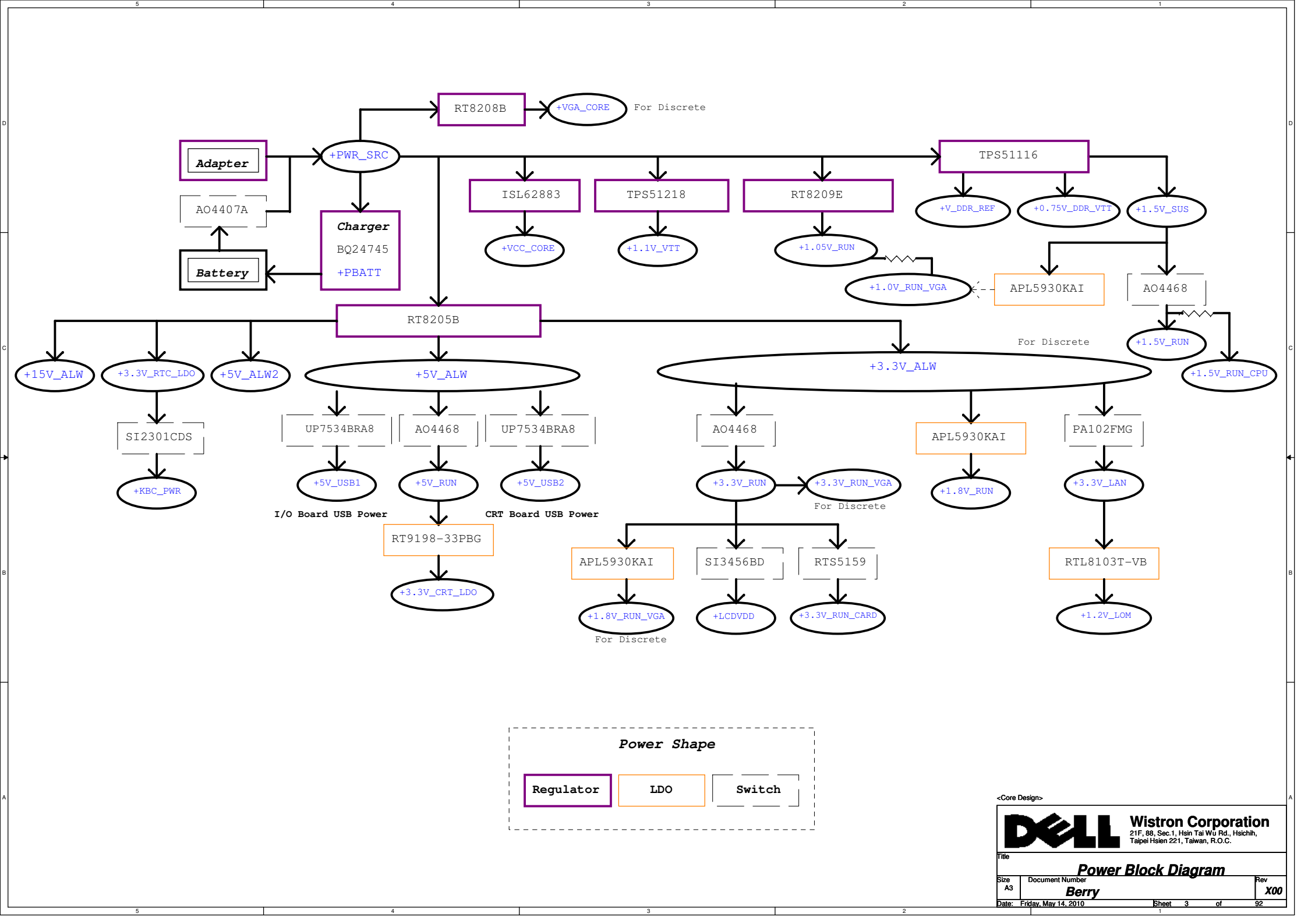
CPU DC/DC ISL62883 47	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE
SYSTEM DC/DC TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.1V_VTT
SYSTEM DC/DC RT8205B 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW
SYSTEM DC/DC TPS51116 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF
SYSTEM DC/DC RT8209E 48	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_RUN
VGA RT8208B 89	
INPUTS	OUTPUTS
+PWR_SRC	+VGA_CORE
TI CHARGER BQ24745 45	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC
SYSTEM DC/DC APL5930 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN +1.8V_RUN_VGA
SYSTEM DC/DC APL5930 90	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.0V_RUN_VGA
Switches	
INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN
PCB LAYER	
L1:Top L2:VCC L3:Signal L4:Signal L5:GND L6:Bottom	

<Core Design>

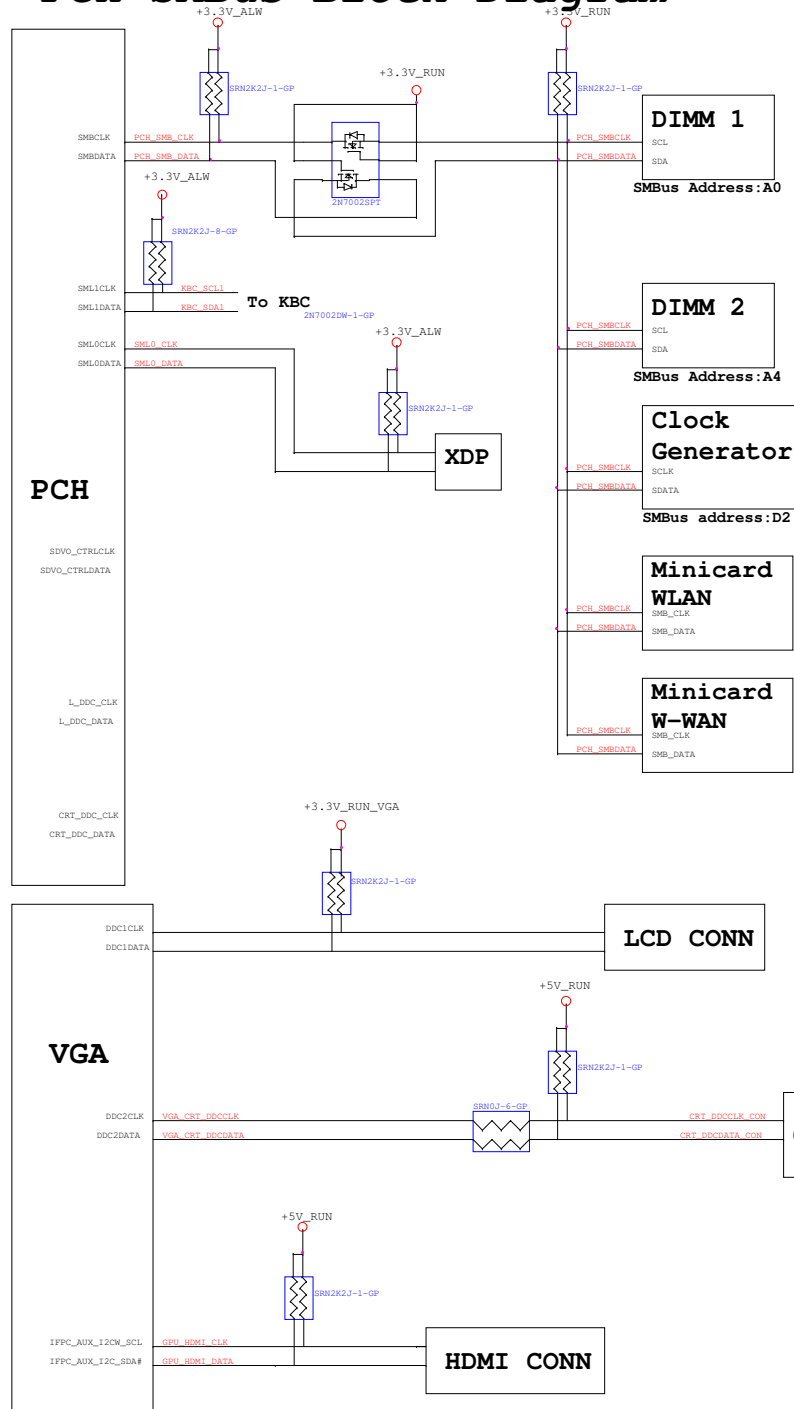


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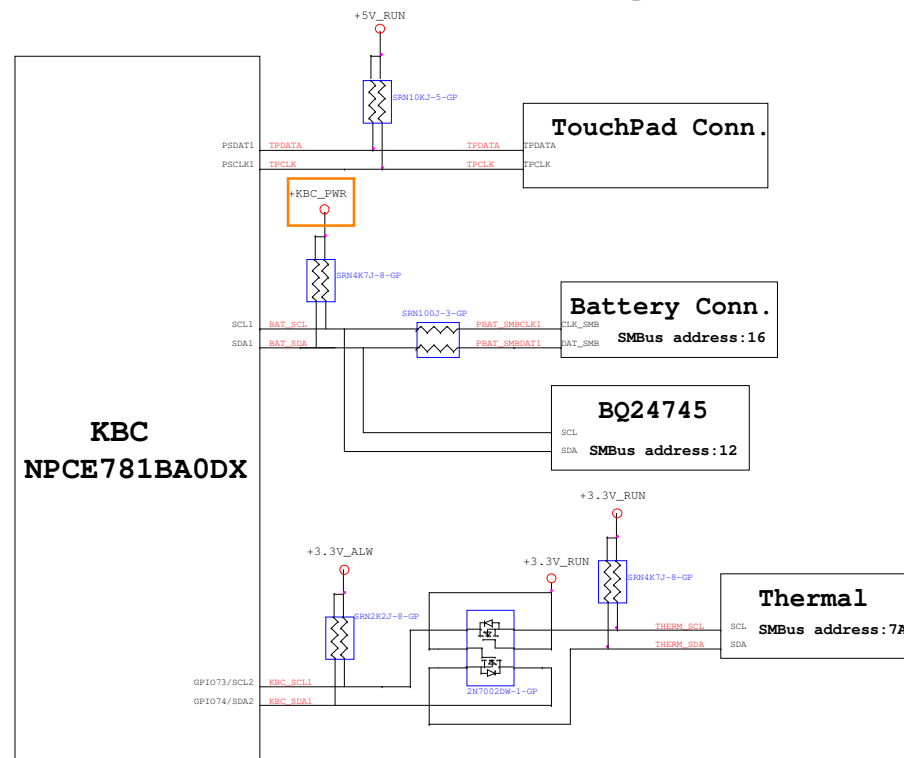
Title <b>Block Diagram</b>		
Size A3	Document Number <b>Berry</b>	Rev <b>X00</b>
Date: Friday, May 14, 2010	Sheet 2 of 92	



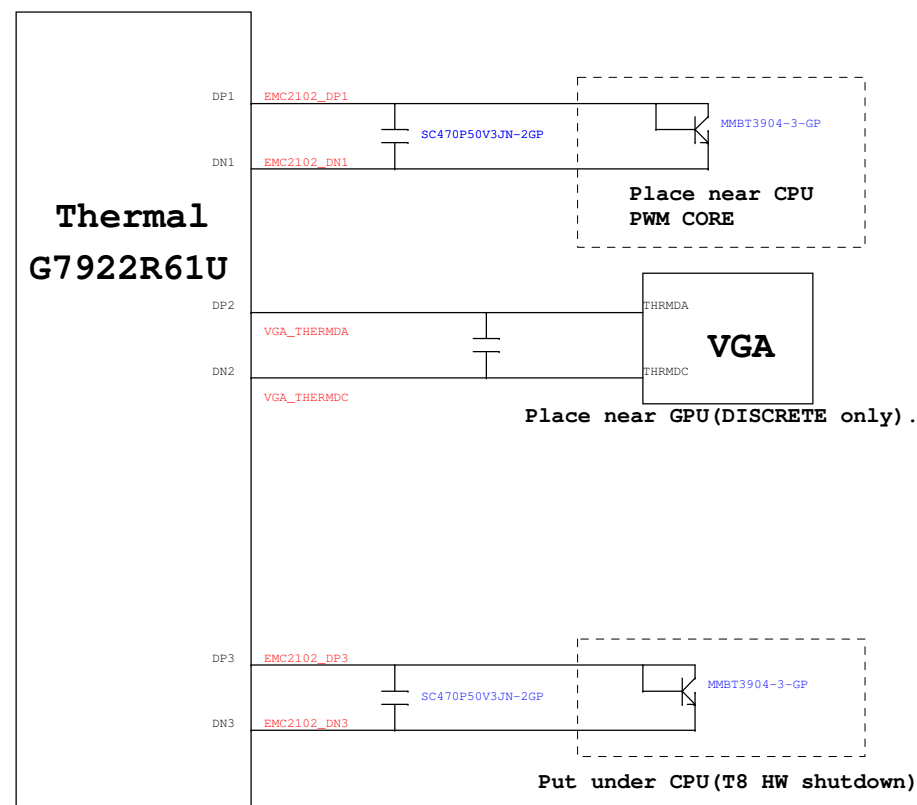
# PCH SMBus Block Diagram



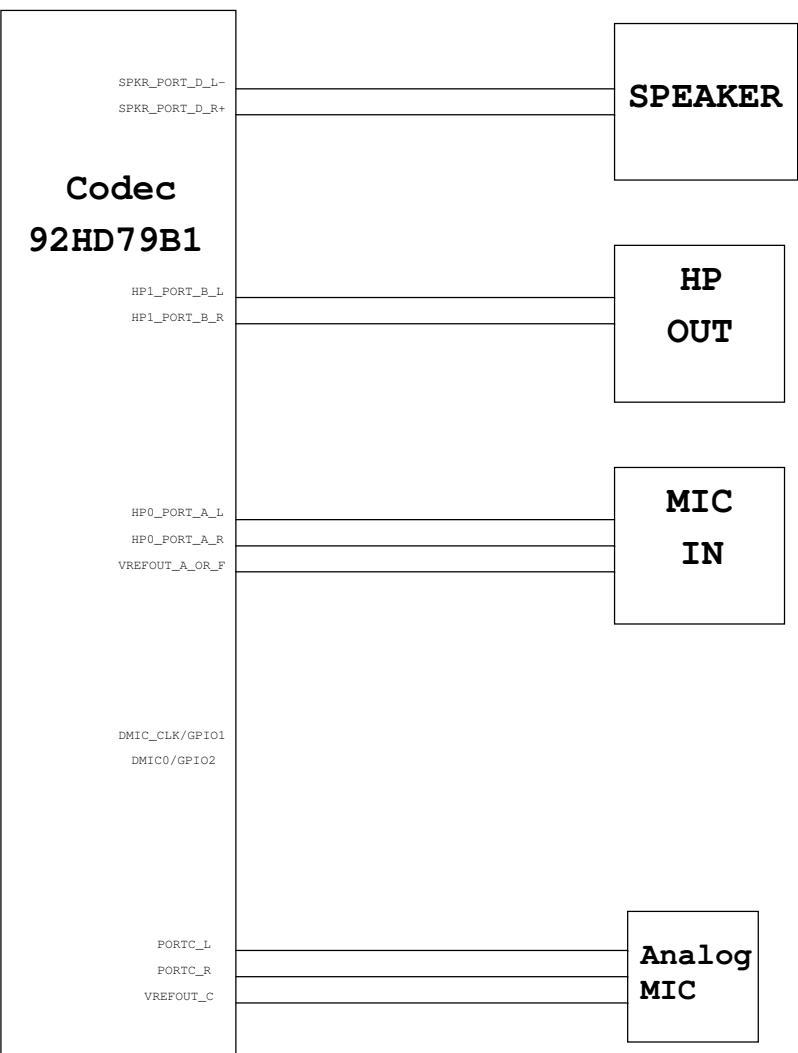
# KBC SMBus Block Diagram



# Thermal Block Diagram



# Audio Block Diagram



## PCH Strapping

Calpella Schematic Checklist Rev.0\_7

Name	Schematics Notes
SPKR	<b>Reboot option at power-up</b> <b>Default Mode:</b> Internal weak Pull-down. <b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	<b>Default Mode:</b> Internal pull-up. <b>Low (0) = Top Block Swap Mode</b> (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	<b>High (1) = Integrated VRM is enabled</b> <b>Low (0) = Integrated VRM is disabled</b>
GNT0#, GNT1#/GPIO51	<b>Default (SPI):</b> Left both GNT0# and GNT1# floating. No pull up required. <b>Boot from PCI:</b> Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. <b>Boot from LPC:</b> Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	<b>Default - Internal pull-up.</b> <b>Low (0) =</b> Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	<b>Default:</b> Do not pull low. <b>Disable ME in Manufacturing Mode:</b> Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	<b>Enable iTPM:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. <b>Disable iTPM:</b> Left floating, no pull-down required.
NV_ALE	<b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. <b>Disable Danbury:</b> Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	<b>Low (0):</b> Flash Descriptor Security will be overridden. <b>High (1) :</b> Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	<b>Default = Do not connect (floating)</b> <b>High(1) =</b> Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. <b>Low (0) =</b> Disables the VccVRM. Need to use on-board filter circuits for analog rails.

## PCIE Routing

LANE1	RESERVED
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	W-WAN
LANE5	RESERVED
LANE6	RESERVED
LANE7	H55/HM55 no support
LANE8	H55/HM55 no support

## USB Table

USB	
Pair	Device
0	USB2 (CRT Board)
1	USB3 (CRT Board)
2	WLAN (I/O Board)
3	RESERVED
4	CARD READER
5	BLUETOOTH
6	HM55 no support
7	HM55 no support
8	USB1 (I/O Board)
9	USB0 (I/O Board ESATA)
10	RESERVED
11	W-WAN (I/O Board)
12	RESERVED
13	CAMERA

## SATA Table

SATA	
Pair	Device
0	HDD
1	ODD
2	HM55 no support
3	HM55 no support
4	ESATA
5	RESERVED

## Processor Strapping

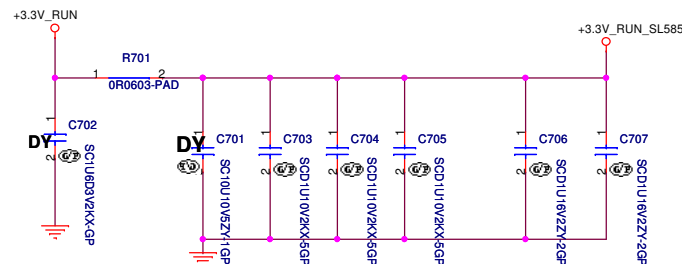
Calpella Schematic Checklist Rev.0\_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	<b>Embedded DisplayPort Presence</b>	<b>1:</b> Disabled - No Physical Display Port attached to Embedded DisplayPort. <b>0:</b> Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	<b>PCI-Express Static Lane Reversal</b>	<b>1:</b> Normal Operation. <b>0:</b> Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	<b>PCI-Express Configuration Select</b>	<b>1:</b> Single PCI-Express Graphics <b>0:</b> Bifurcation enabled	1
CFG[7]	<b>Reserved - Temporarily used for early Clarksfield samples.</b>	<b>Clarksfield (only for early samples pre-ES1) -</b> Connect to GND with 3.01K Ohm/5% resistor <b>Note:</b> Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

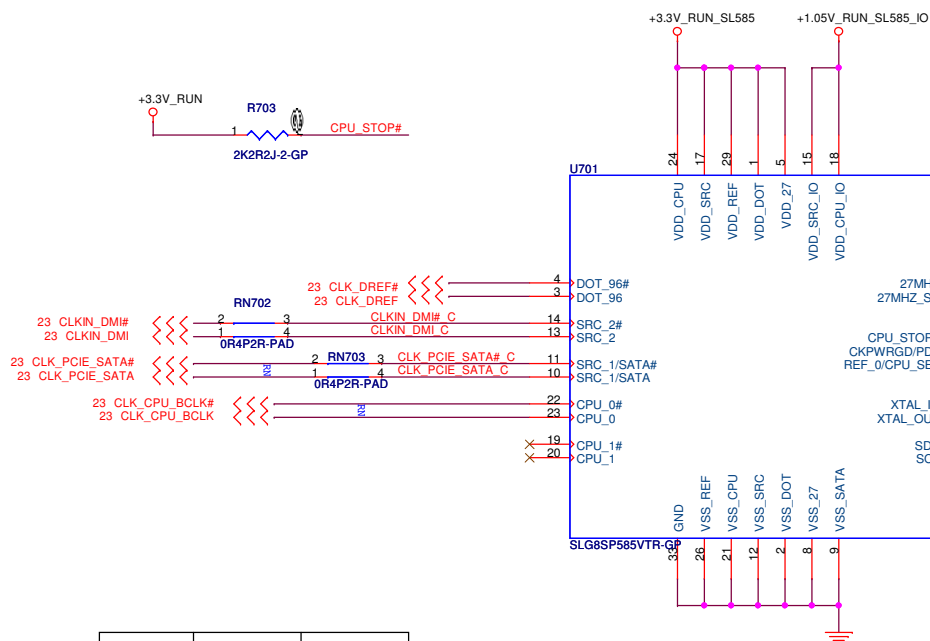
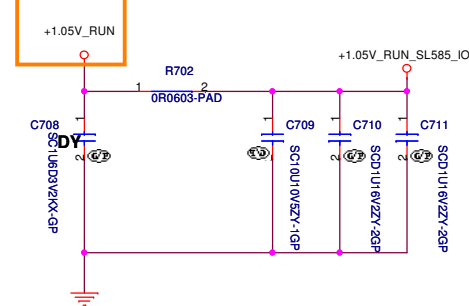
<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b><i>Table of Content</i></b>			
Size A3	Document Number <b><i>Berry</i></b>	Rev <b><i>X00</i></b>	
Date: Friday, May 14, 2010	Sheet 6	of	92

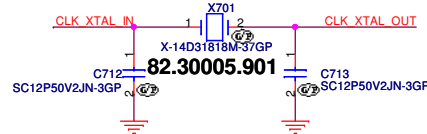
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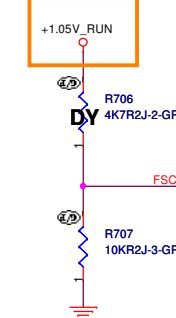
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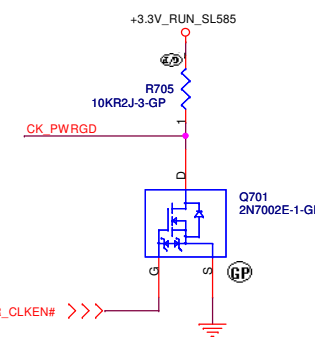
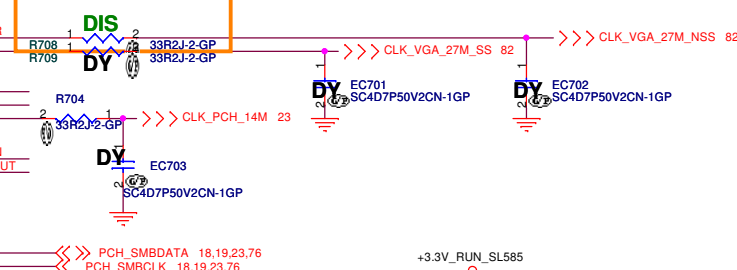
FSC	0	1
SPEED	133MHz (Default)	100MHz



CFD-20100423



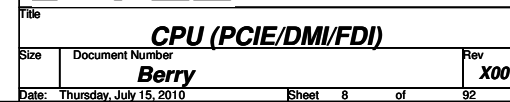
CFD\_X00\_20100503



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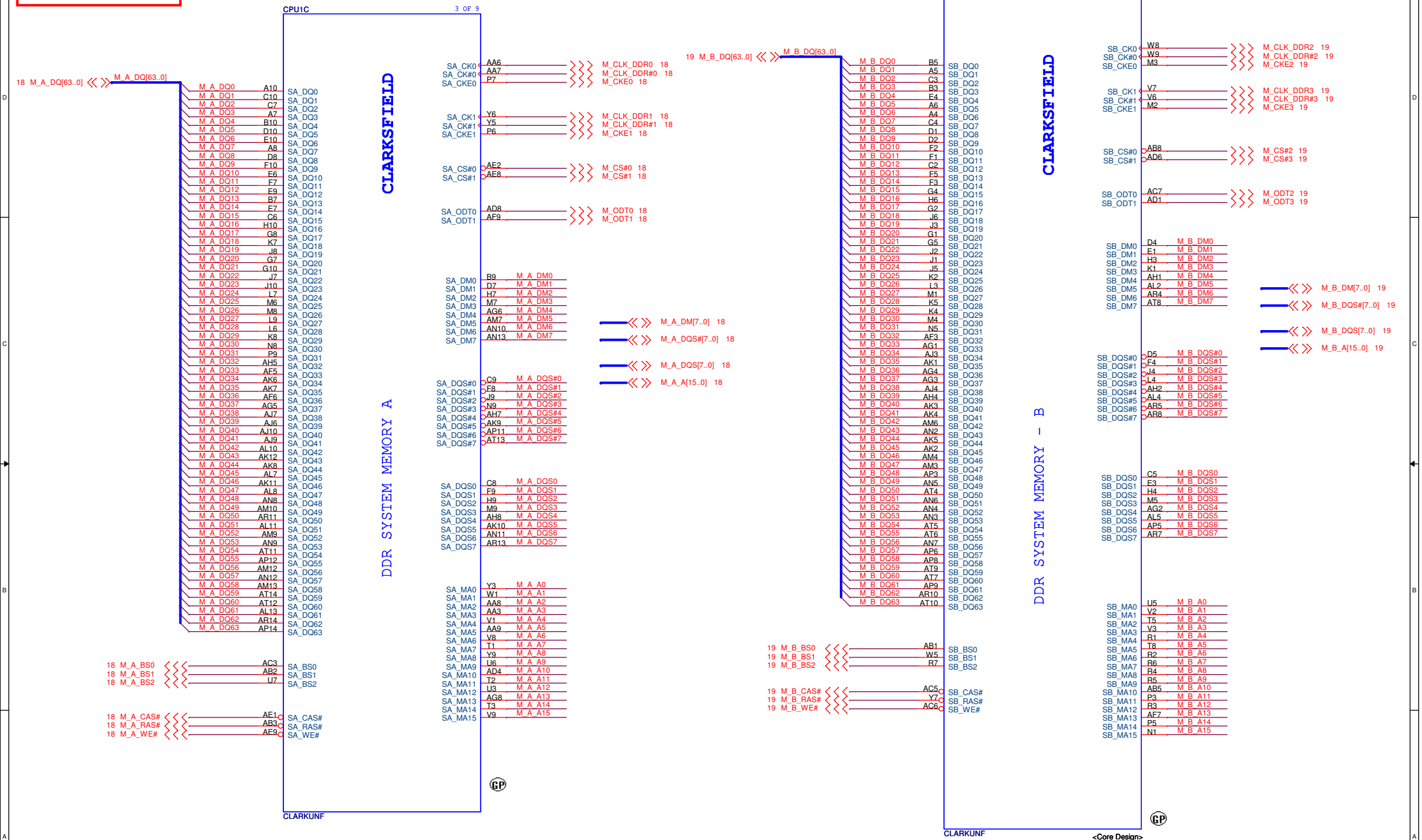
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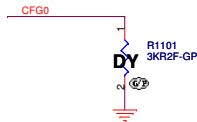
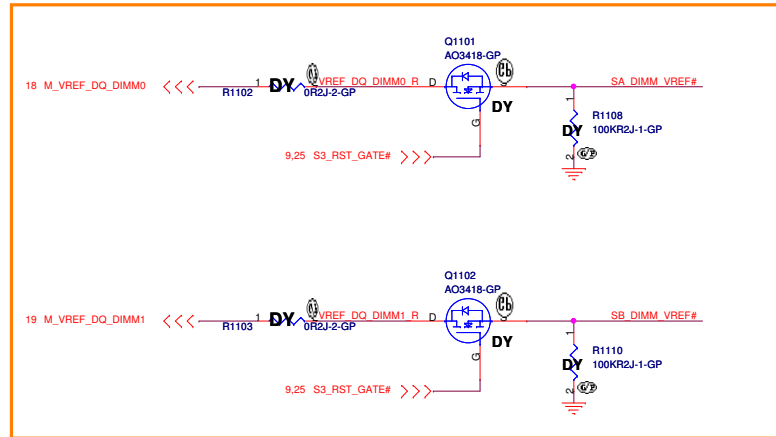




**SSID = CPU**

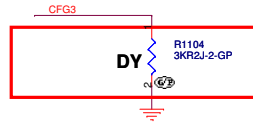


CFD-20100512

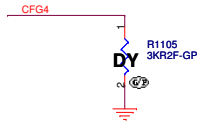


PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

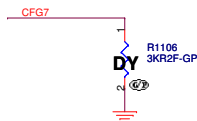
CFD-A00\_20100715



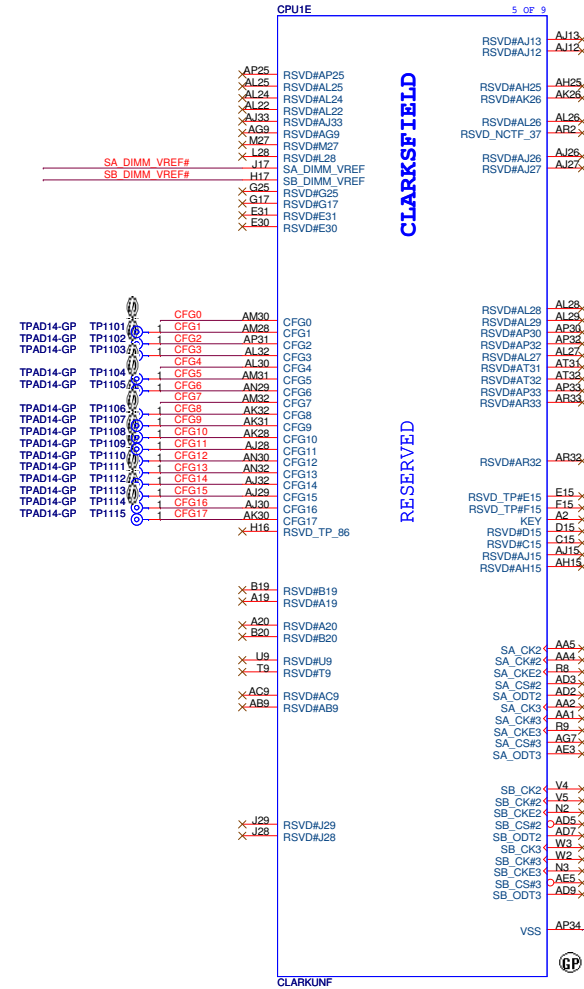
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled: No Physical Display Port attached to Embedded Display Port 0:Enabled: An external Display Port device is connected to the Embedded Display Port

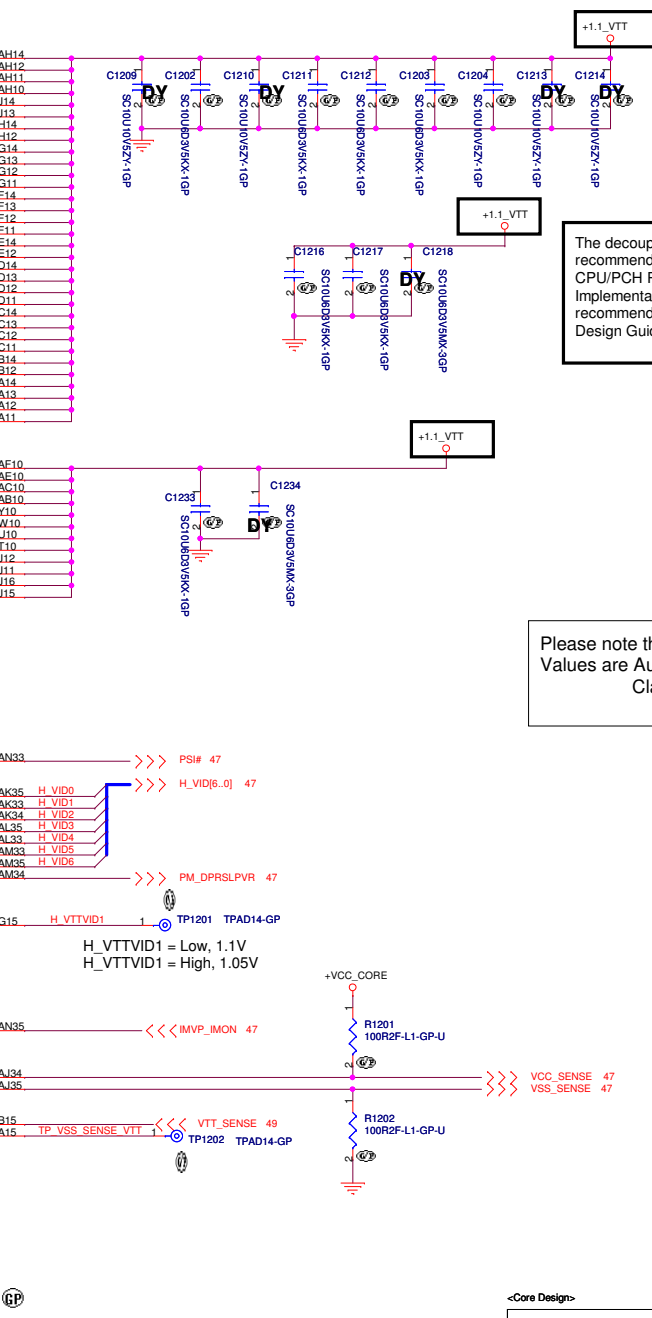
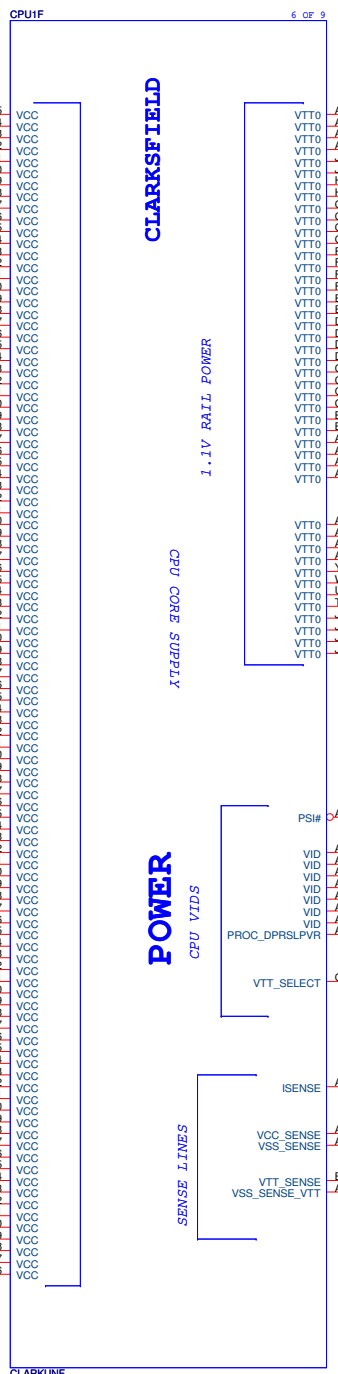
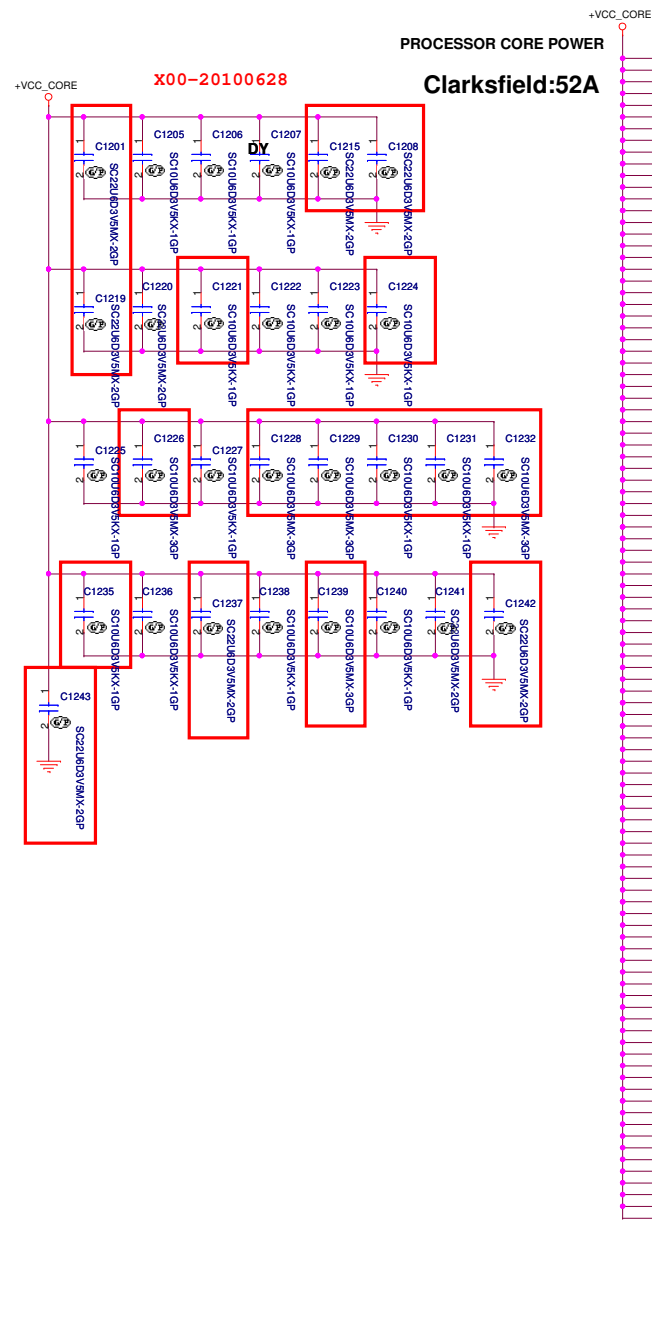


CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.  Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

SSID = CPU



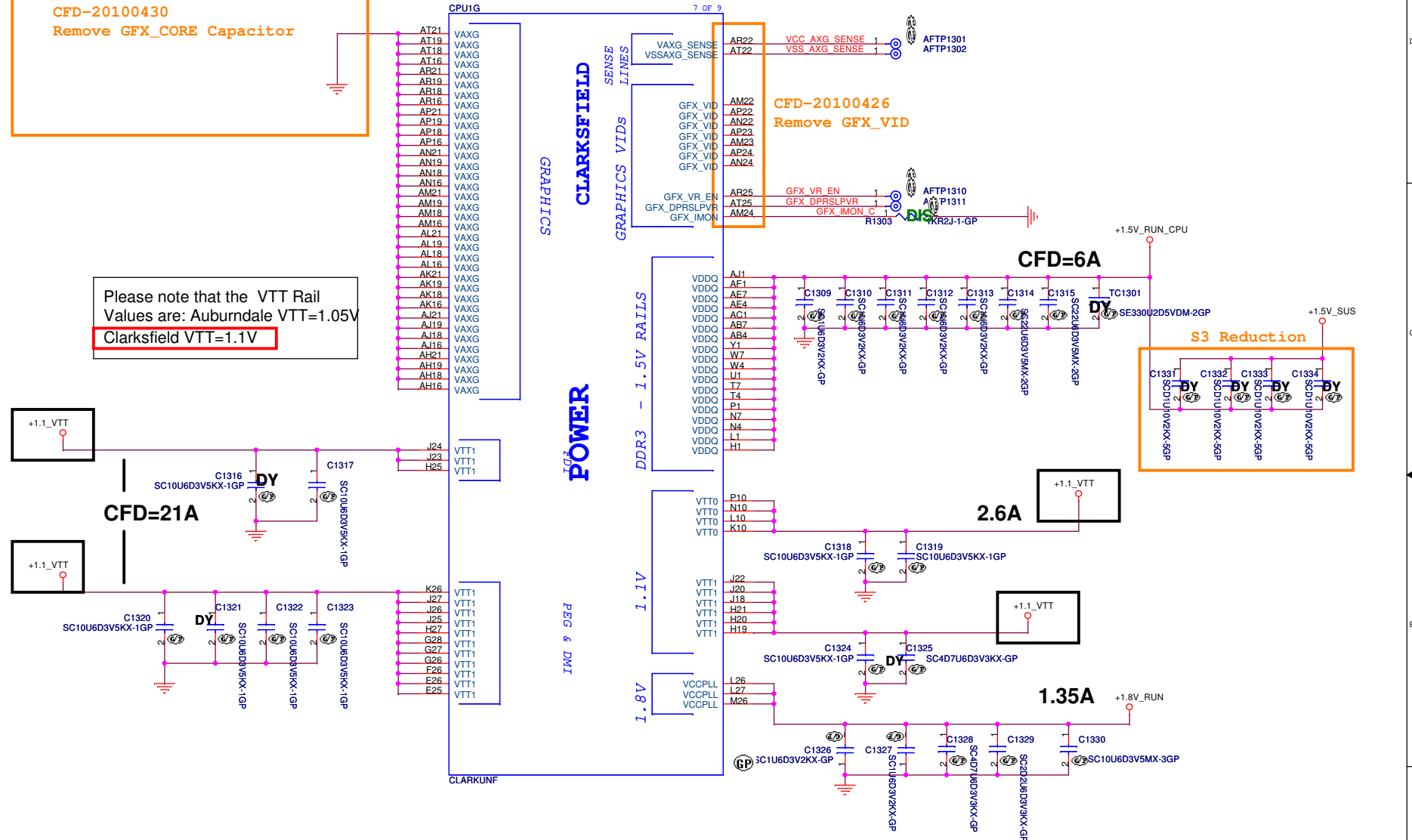
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V  
Clark'sfield VTT=1.1V

**SSID = CPU**

CFD-20100430  
Remove GFX\_CORE Capacitor

Please note that the VTT Rail  
Values are: Auburndale VTT=1.05V  
Clarksfield VTT=1.1V



## <Core Design>



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Title

**CPU (VCC\_GFXCORE)**

Size

Document Number

**Berry**

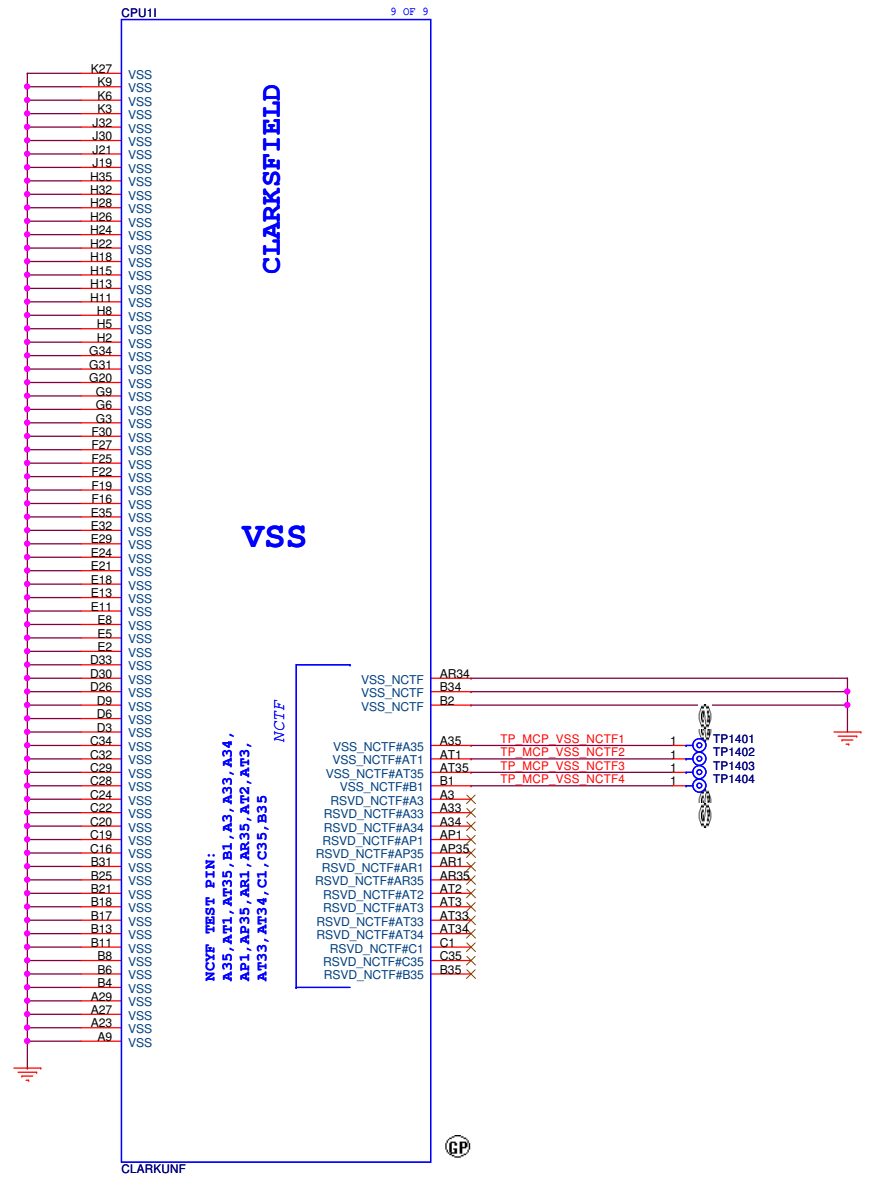
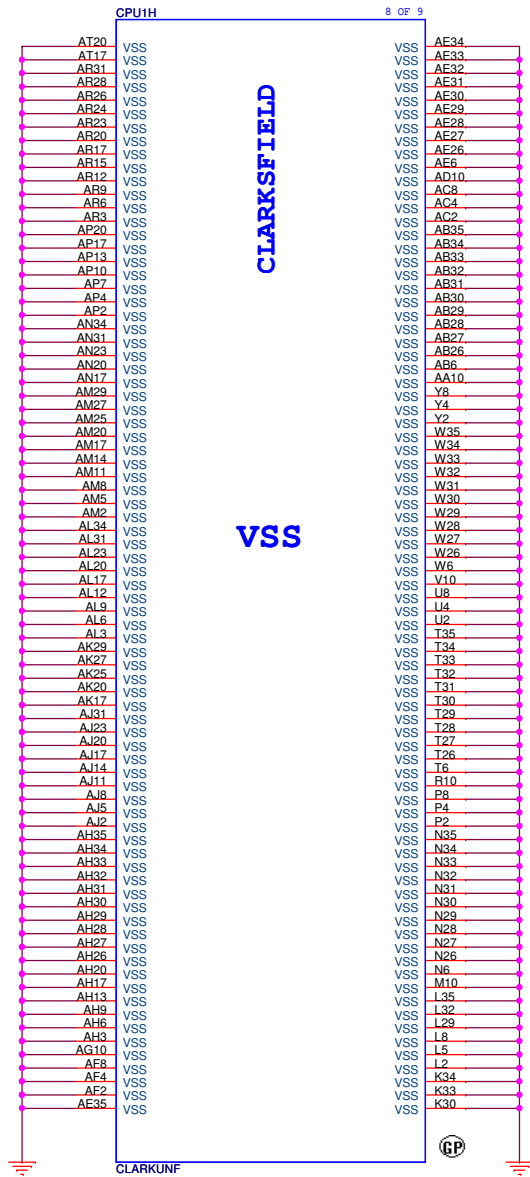
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**X00**

Date: Monday, July 19, 2010

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SSID = CPU



<Core Design>




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Title			CPU (VSS)	
Size	Document Number		Rev	
	Berry		X00	
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Title

Size

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Document Number

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Title

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Document Number  
**Berry**

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**X00**

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Reserved



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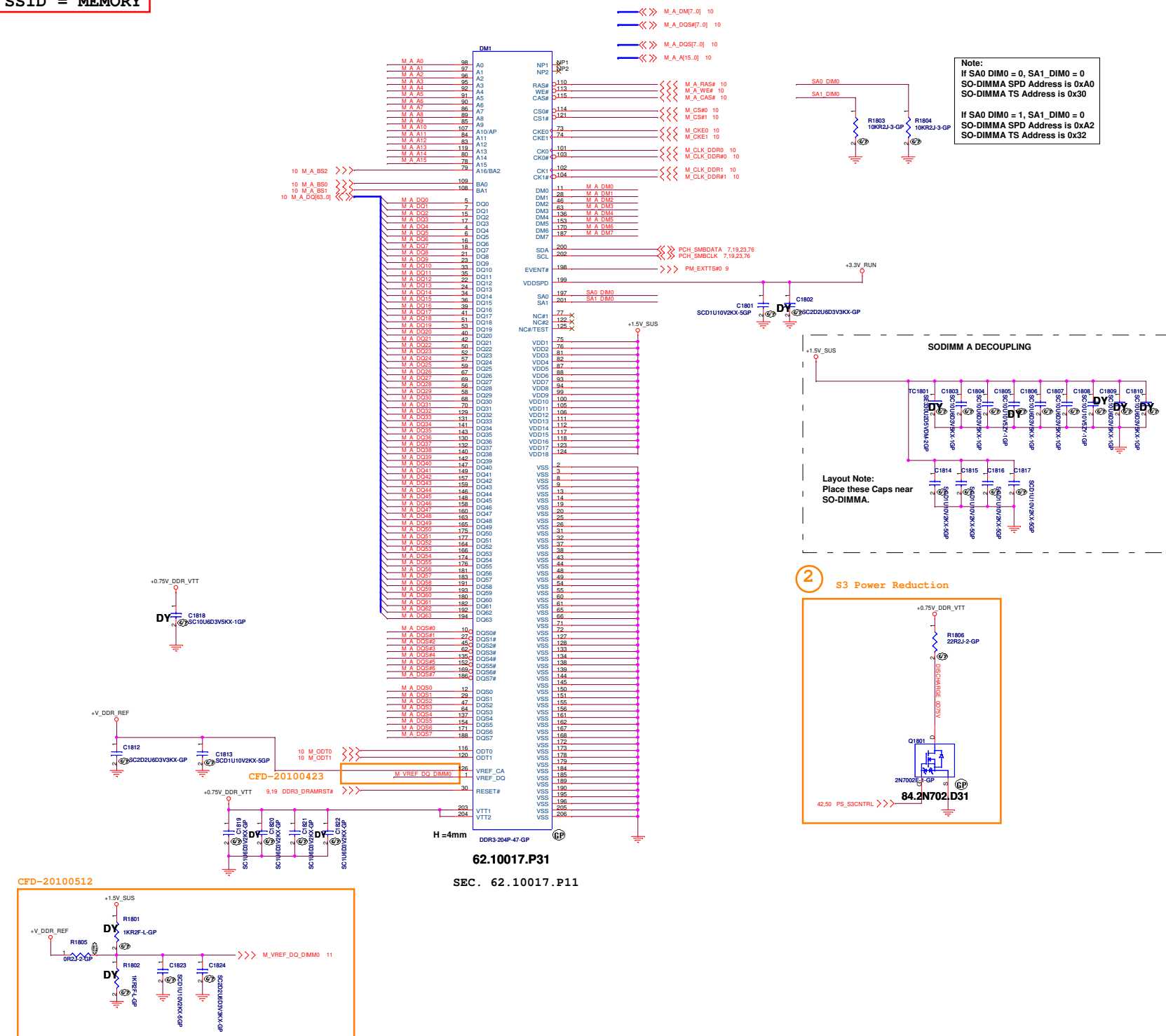
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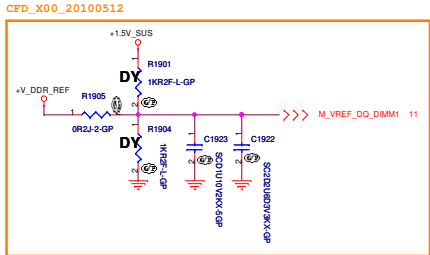
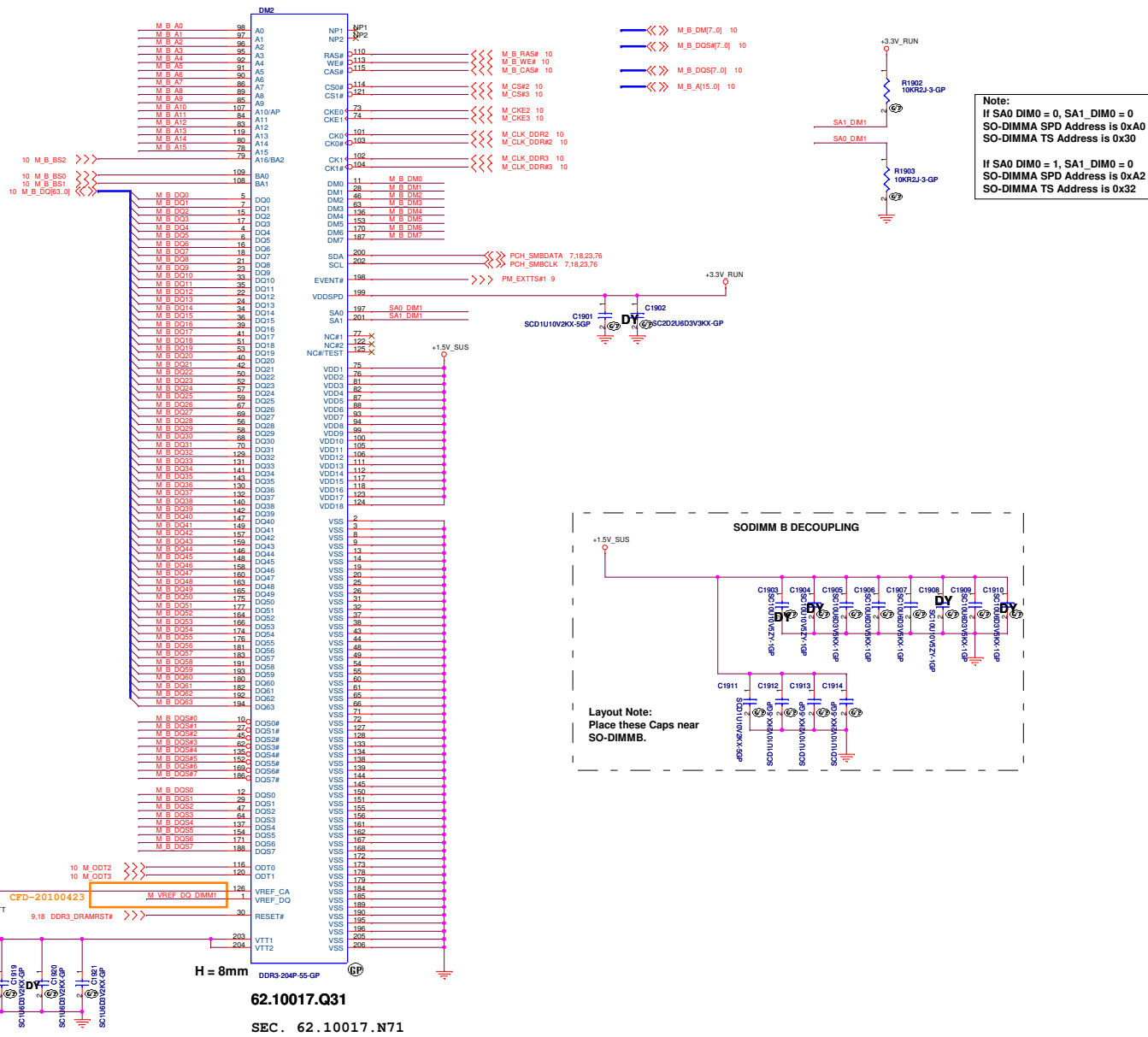
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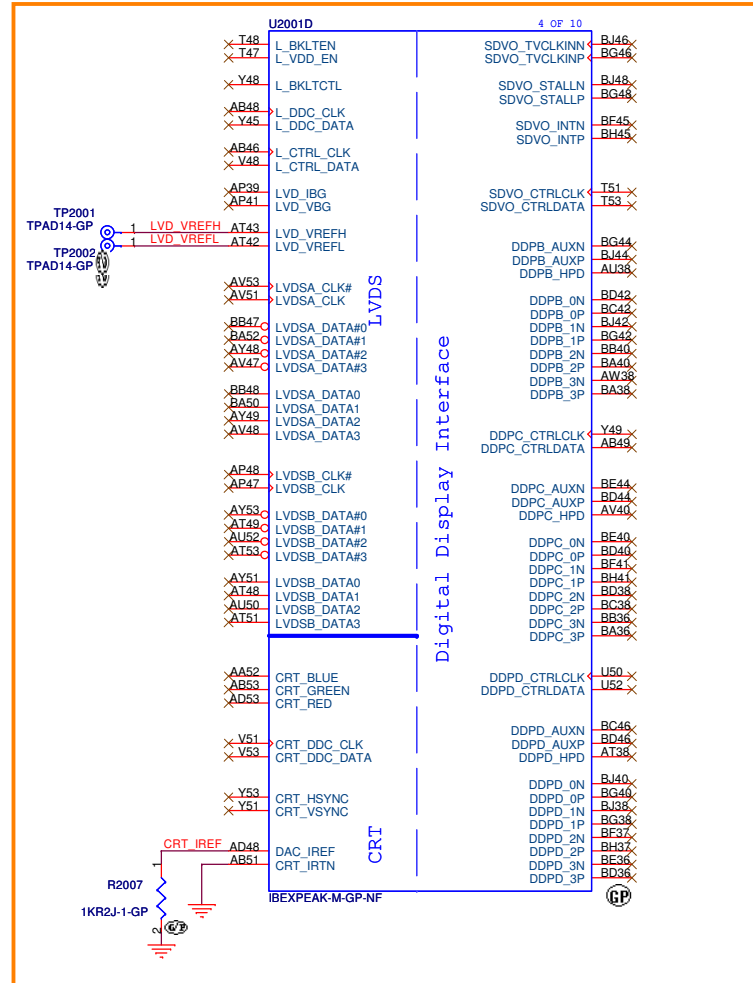
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SSID = MEMORY



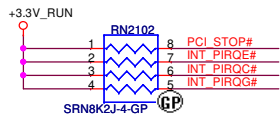
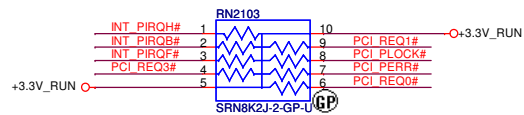
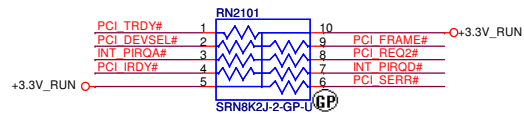
CFD-20100511  
For DG2.1 p.208



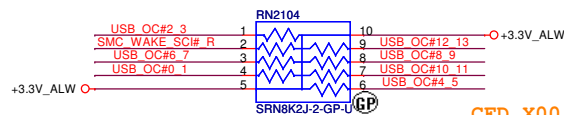
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Title <b>PCH (LVDS/CRT/DDI)</b>			
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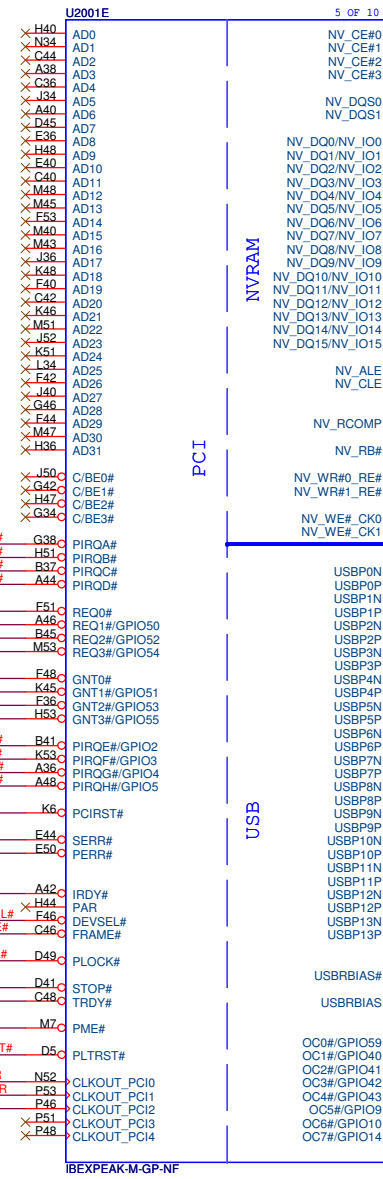
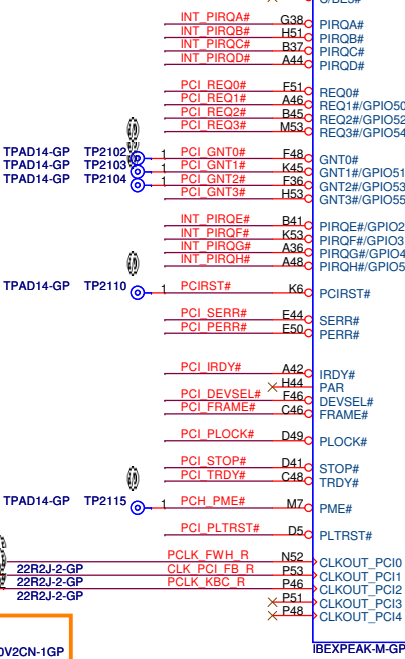
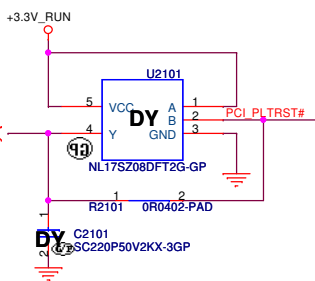
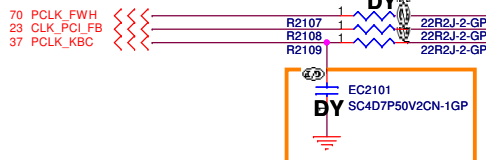
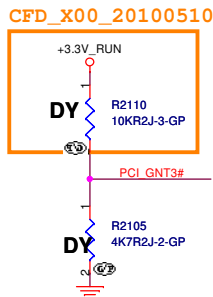
SSID = PCH



BOOT BIOS Strap		
PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI (Default)



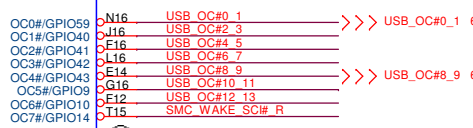
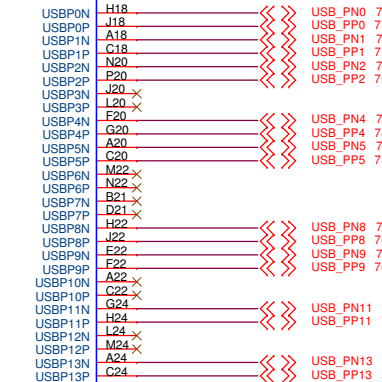
A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



NVRAM

PCI

USB



DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

Danbury Technology:  
Disabled when Low.  
Enable when High.

USB	
Pair	Device
0	USB2 (CRT Board)
1	USB3 (CRT Board)
2	WLAN (I/O Board)
3	X
4	CARD READER
5	BLUETOOTH
6	X
7	X
8	USB1 (I/O Board)
9	ESATA (I/O Board COMBO)
10	X
11	W-WAN (I/O Board)
12	X
13	CAMERA

<Core Design>

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Title: **PCH (PCI/USB/NVRAM)**

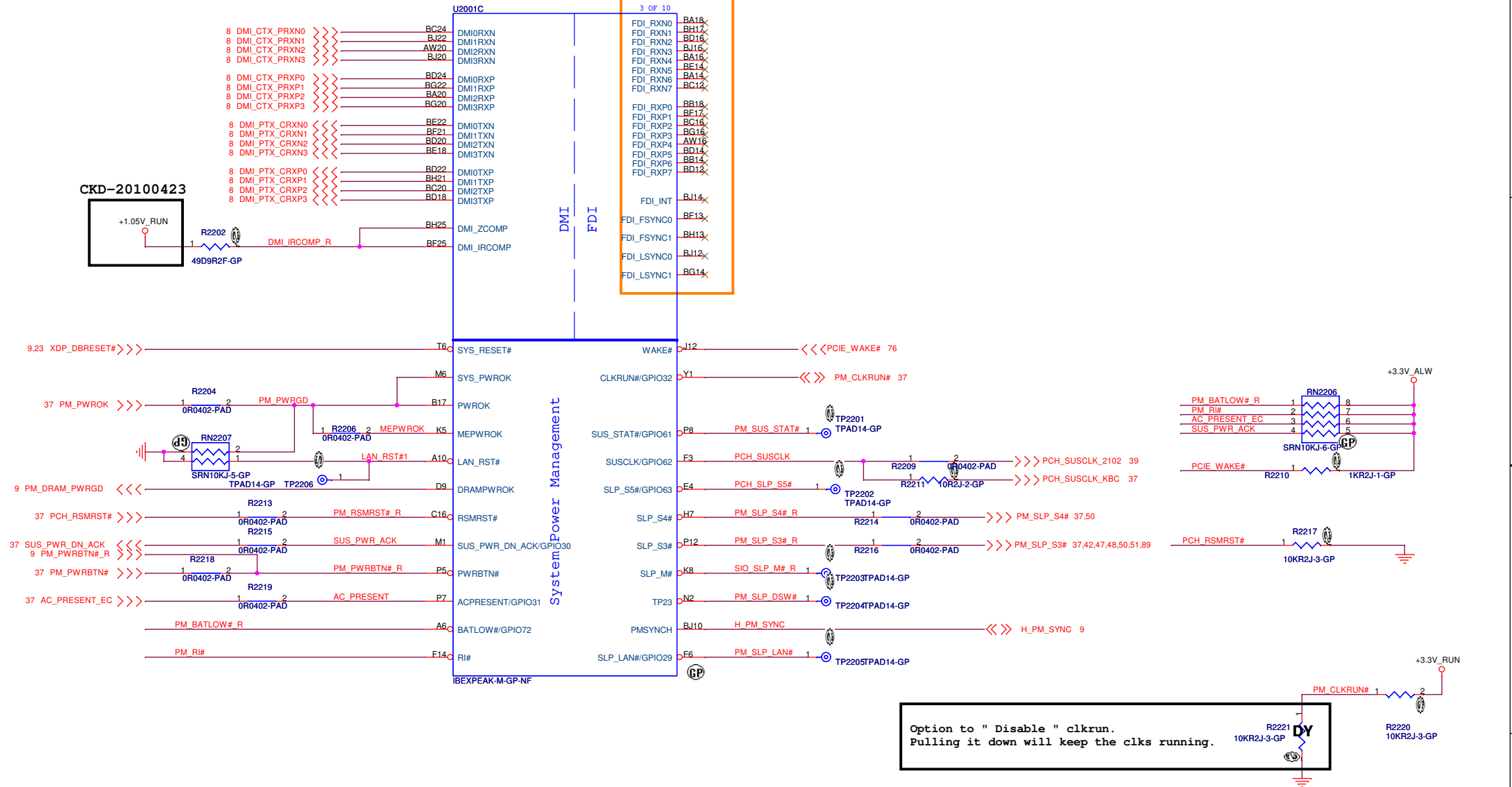
Size: Document Number **Berry** Rev: **X00**

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SSID = PCH

CFD-20100429

CKD-20100423



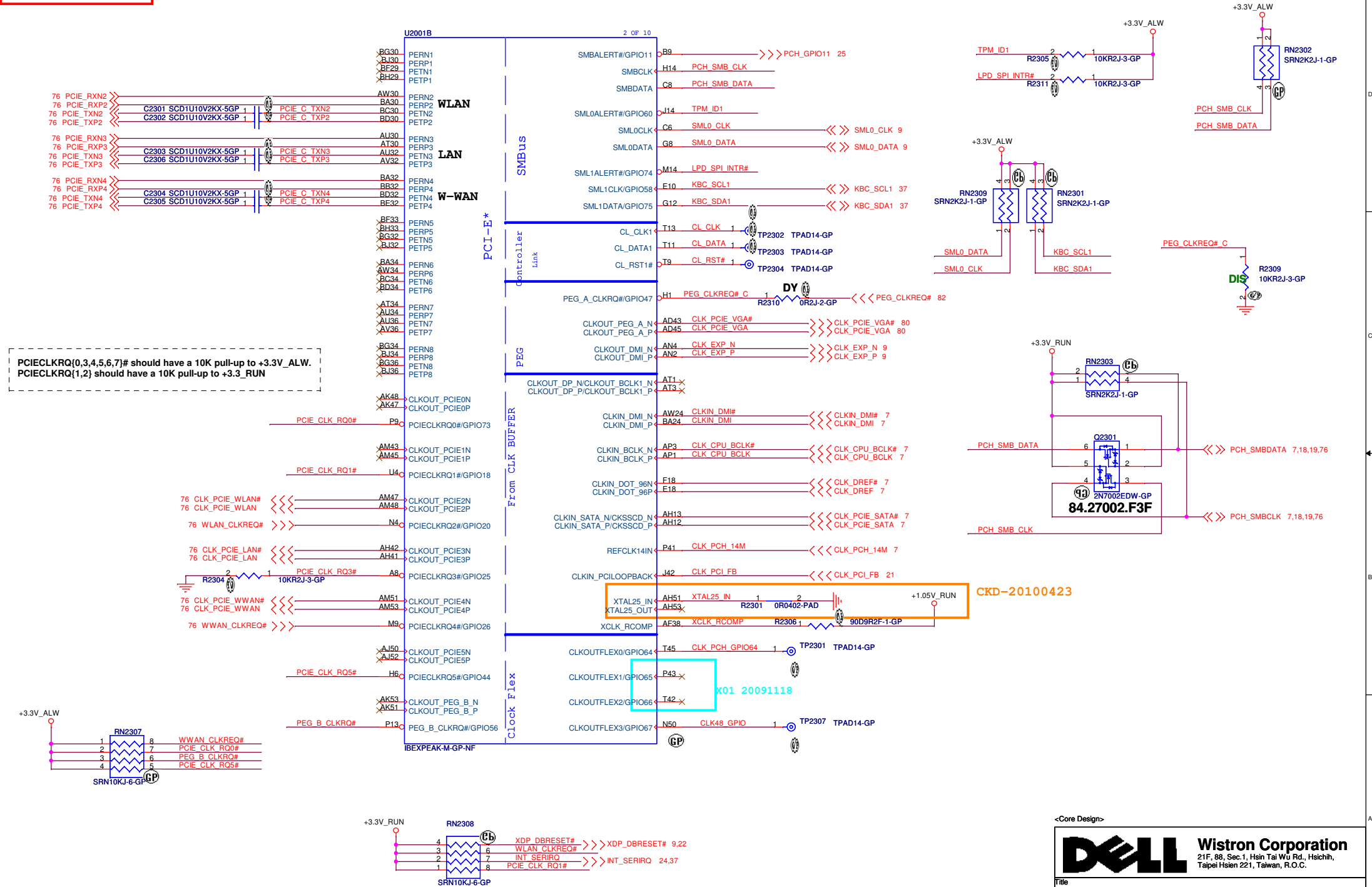
<Core Design>



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Title				
<b>PCH (DM I/FDI/PM)</b>				
Size	Document Number			Rev
	<b>Berry</b>			<b>X00</b>
Date:	Thursday, July 15, 2010		Sheet 22 of	92

**SSID = PCH**



### <Core Design>

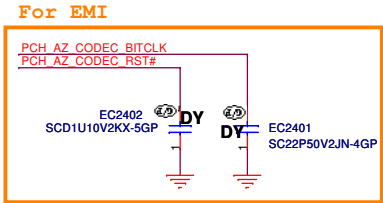
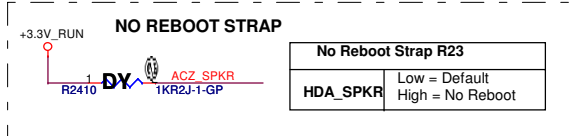
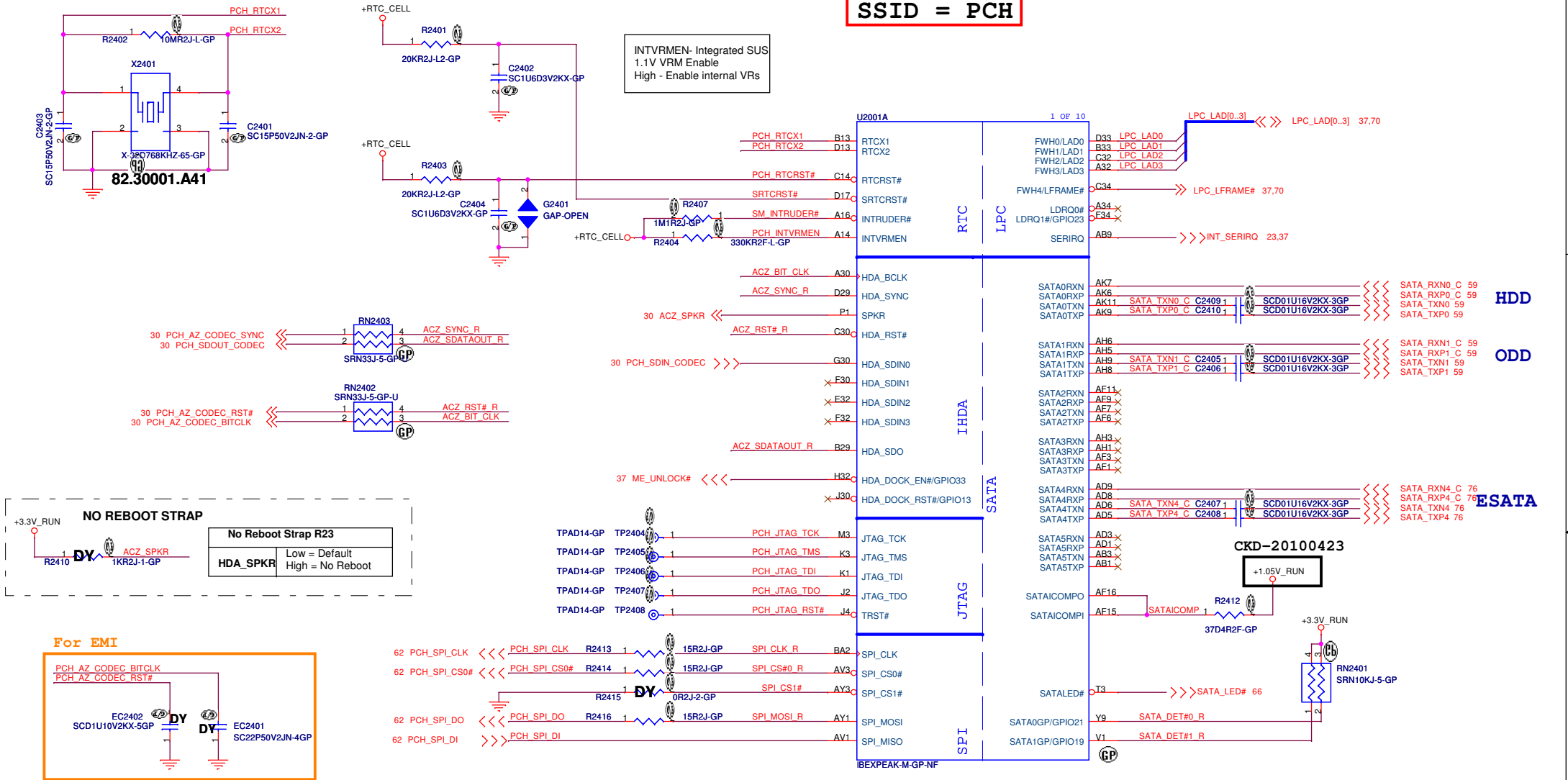


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Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>PCH (PCI-E/SMBUS/CLOCK/CL)</b>			
Size	Document Number	Rev	
	<b>Berry</b>	<b>X00</b>	
Date:	Thursday, July 15, 2010	Sheet	23 of 92

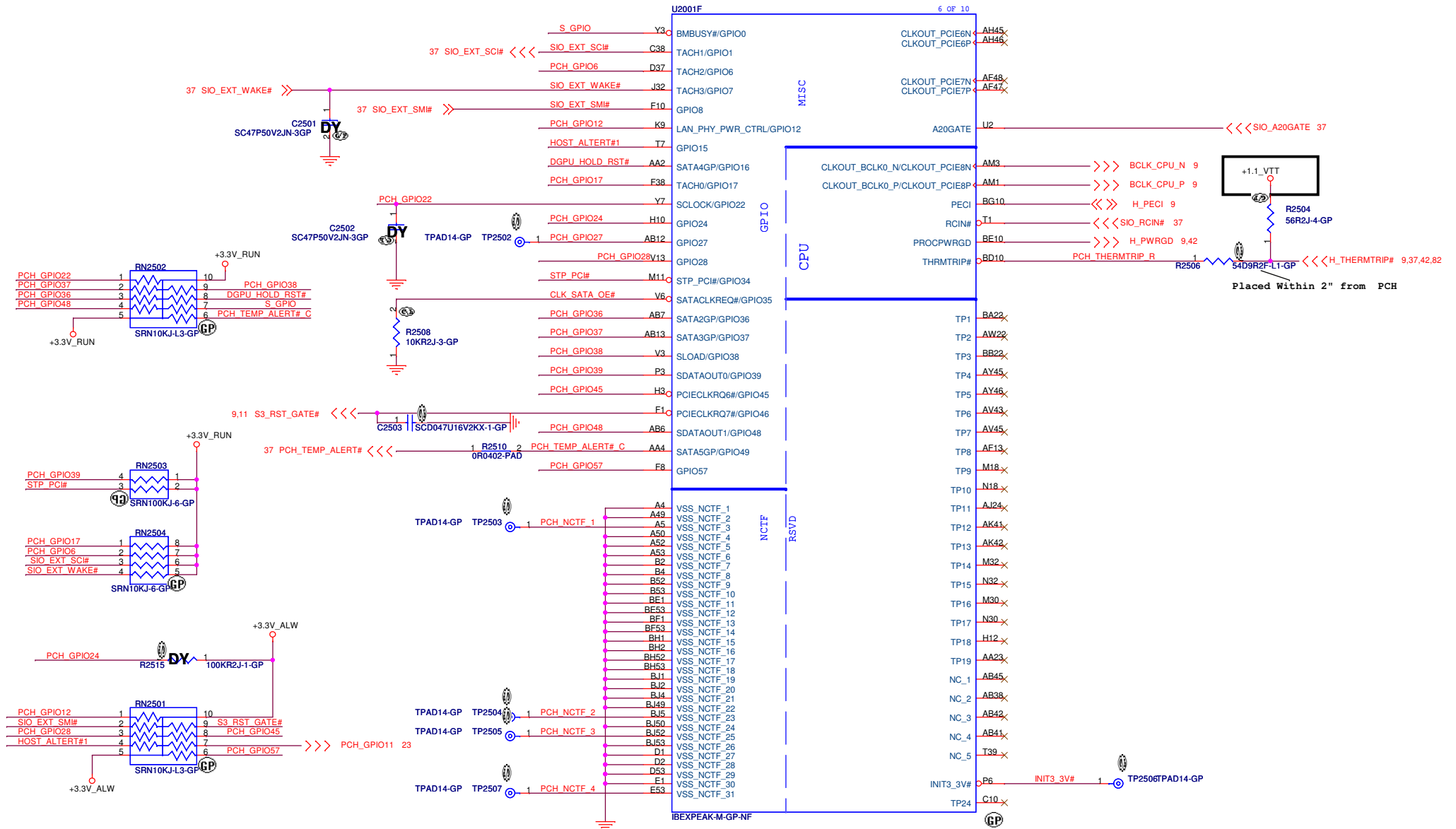
SSID = PCH

INTVRMEN- Integrated SUS  
1.1V VRM Enable  
High - Enable internal VRs





**SSID = PCH**



## <Core Design>



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Title

**PCH (GPIO/CPU)**

Size	Document Number
------	-----------------

**Berry**

Rev  
**X00**

Date: Thursday, July 15, 2010

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SSID = PCH

CKD-20100423

+1.05V\_RUN

1.524A

C2602 SC10U6D3V5KX-1GP  
C2601 SC1U6D3V2KX-GP

+1.05V\_RUN

TP2602

TPAD14-GP VCCAPLLEXP

+1.05V\_RUN

3.208A

C2614 SC1U6D3V5KX-1GP  
C2615 SC1U6D3V2KX-GP  
C2616 SC1U6D3V2KX-GP  
C2617 SC1U6D3V2KX-GP  
C2618 SC1U6D3V2KX-GP

C2621 SCD1U10V2KX-5GP

+3.3V\_RUN

357mA

+1.05V\_RUN

+1.8V\_RUN

R2610 0R0402-PAD  
TP2601 VCCFDIPLL  
TPAD14-GP

VCCAFDI\_VRM

VCCFDIPLL

VCCIO

U2001G  
AB24 VCCCORE  
AB26 VCCCORE  
AB28 VCCCORE  
AD26 VCCCORE  
AD28 VCCCORE  
AF26 VCCCORE  
AF28 VCCCORE  
AF30 VCCCORE  
AF31 VCCCORE  
AH26 VCCCORE  
AH28 VCCCORE  
AH30 VCCCORE  
AH31 VCCCORE  
AJ30 VCCCORE  
AJ31 VCCCORE  
AK24 VCCIO  
BJ24 VCCAPLLEXP  
AN20 VCCIO  
AN22 VCCIO  
AN23 VCCIO  
AN24 VCCIO  
AN26 VCCIO  
AN28 VCCIO  
BJ26 VCCIO  
BJ28 VCCIO  
AT26 VCCIO  
AU26 VCCIO  
AV26 VCCIO  
AW26 VCCIO  
BA26 VCCIO  
BA28 VCCIO  
BB26 VCCIO  
BB28 VCCIO  
BC26 VCCIO  
BC28 VCCIO  
BD26 VCCIO  
BE26 VCCIO  
BE28 VCCIO  
BG26 VCCIO  
BH27 VCCIO  
AN30 VCCIO  
AN31 VCCIO  
AN35 VCC3\_3  
AT22 VCCVRM[1]  
BJ18 VCCFDIPLL  
AM23 VCCIO  
IBEXPEAK-M-GP-NF

POWER

VCC CORE

CRT

LVDS

HVCMOS

DMI

PCI E\*

NAND / SPI

FDI

7 OF 10

VCCADAC

VCCADAC

VSSA\_DAC

VSSA\_DAC

VCCALVDS

VSSA\_LVDS

VCCTX\_LVDS

VCCTX\_LVDS

VCCTX\_LVDS

VCCTX\_LVDS

VCC3\_3

VCC3\_3

VCC3\_3

VCCVRM

VCCDMI

VCCDMI

VCCPNAND

VCCPNAND

VCCPNAND

VCCPNAND

VCCPNAND

VCCPNAND

VCCPNAND

VCCPNAND

VCCPNAND

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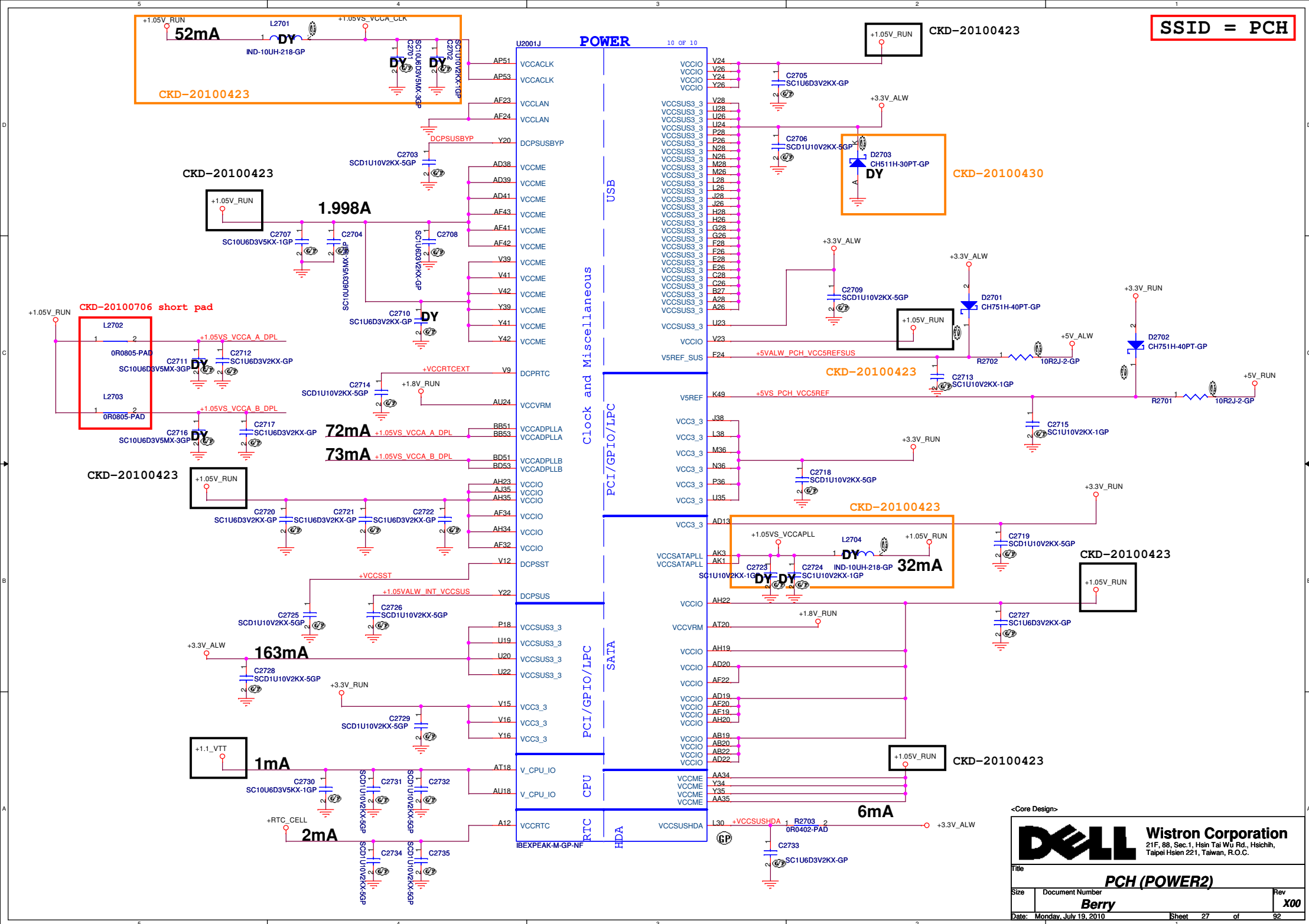
VCCPNAND

VCCPNAND

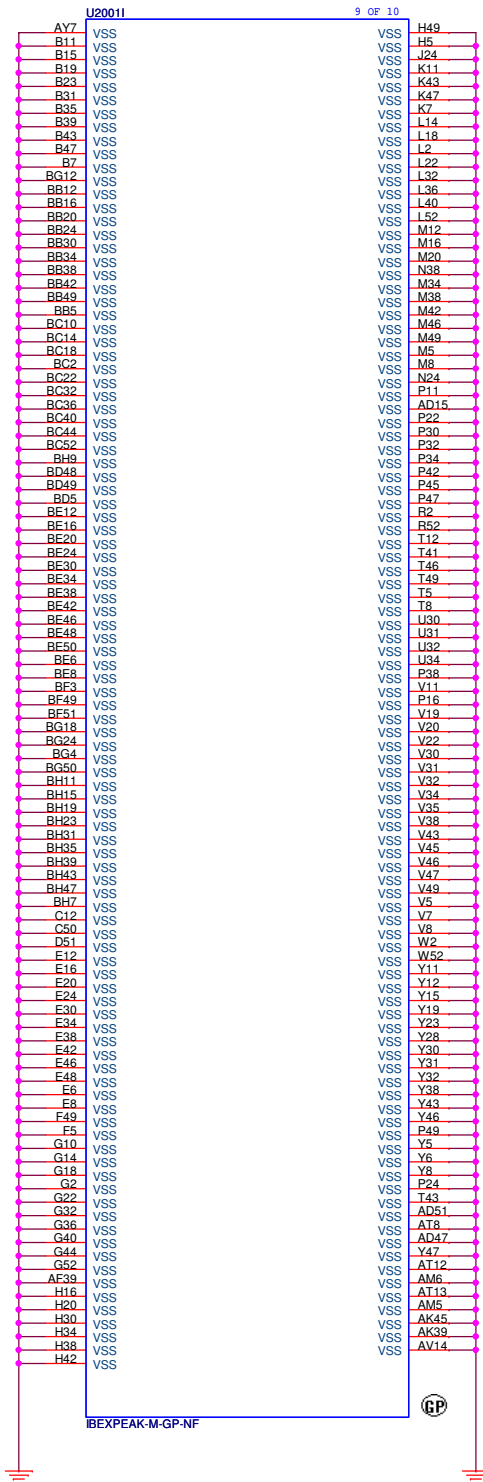
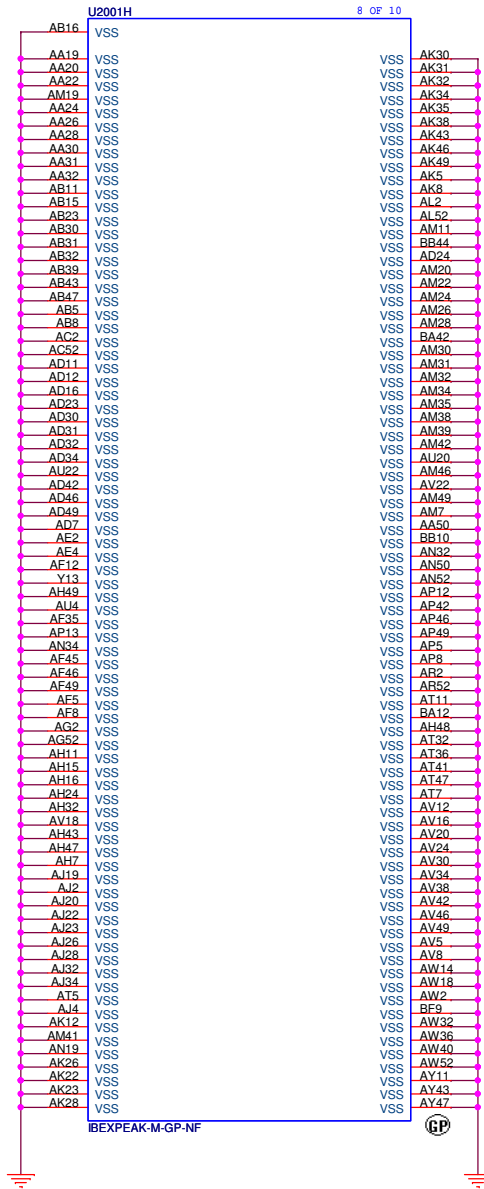
VCCPNAND

VCCPNAND

VCCPNAND



**SSID = PCH**



## <Core Design>



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Title

**PCH (VSS)**

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size  
A3

Document Number  
**Berry**

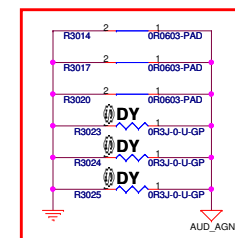
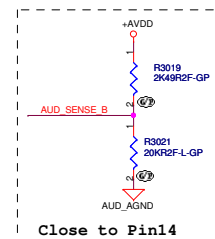
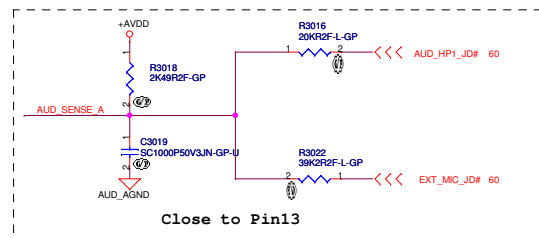
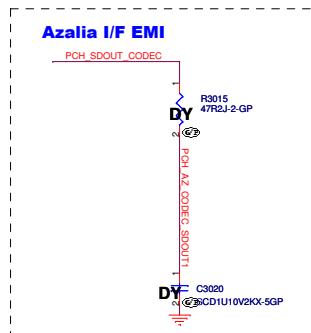
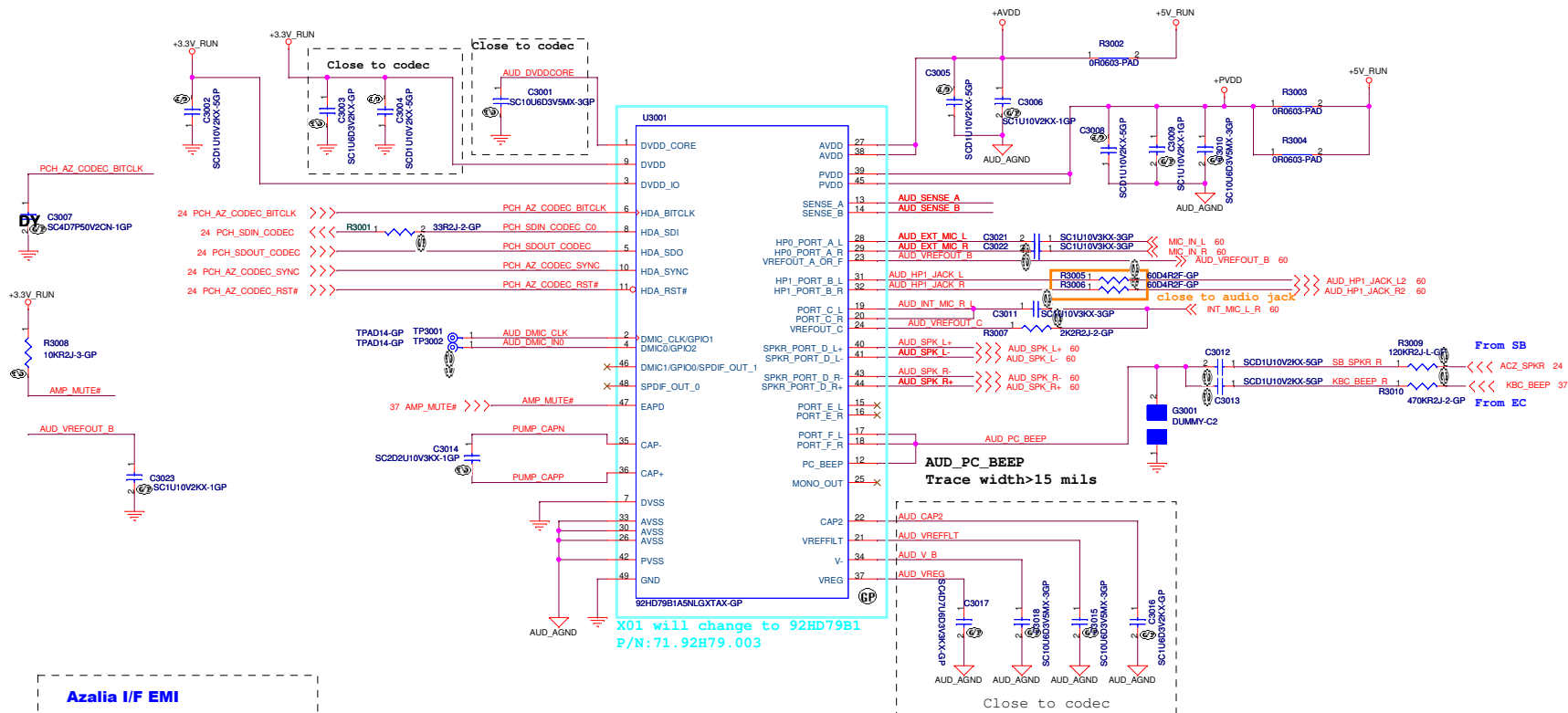
Date: Friday, May 14, 2010

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SSID = AUDIO



DG15 CFD\_X00\_20100628  
connect to clear GND

(Blanking)

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Title

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<Core Design>

DELL

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Title

Size

Document Number

Rev

Custom

**Berry**

**X00**


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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

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<Core Design>



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Title

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Date: Friday, May 14, 2010	Sheet 34 of 92	

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<Core Design>



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<Core Design>



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Title

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A3

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**X00**

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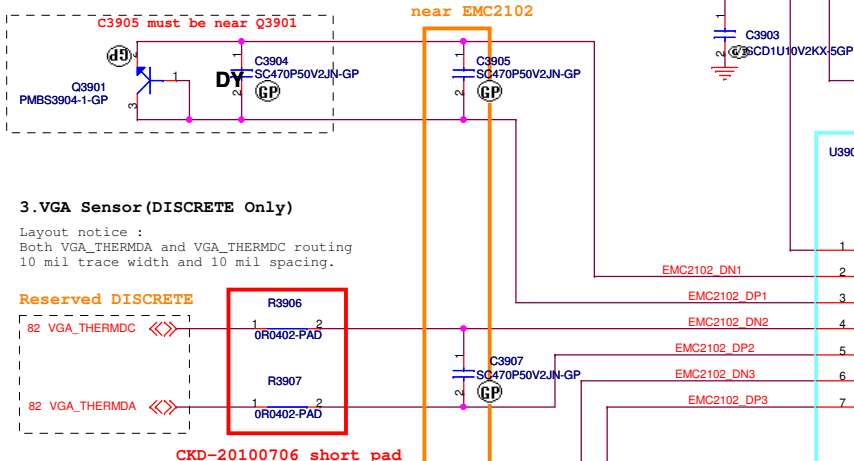
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		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b><i>Reserved</i></b>			
Size A4	Document Number		Rev <b><i>X00</i></b>
Date: Friday, May 14, 2010		Sheet 38 of	92

# SSID = Thermal

## 1. Place near CPU PWM CORE and PCH.

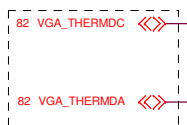
Layout notice :  
Both DN1 and DP1 routing 10 mil trace width and 10 mil spacing.



## 3.VGA Sensor(DISCRETE Only)

Layout notice :  
Both VGA\_THERMDA and VGA\_THERMDC routing 10 mil trace width and 10 mil spacing.

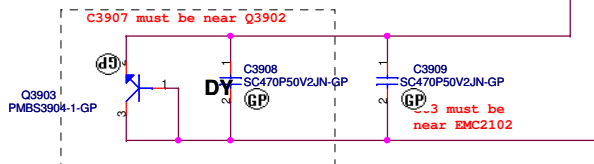
### Reserved DISCRETE



CKD-20100706 short pad

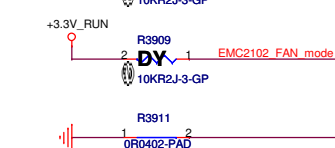
## 4.HW T8 sensor

Layout notice :  
Both DN3 and DP3 routing 10 mil trace width and 10 mil spacing.



GND = Channel 1  
OPEN = Channel 3  
+3.3V = Disabled

GND = Fan is OFF  
OPEN = Fan is at 60% full-scale  
+3.3V = Fan is at 75% full-scale



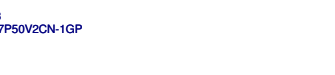
GND = Fan is OFF  
OPEN = Fan is at 60% full-scale  
+3.3V = Fan is at 75% full-scale



GND = Fan is OFF  
OPEN = Fan is at 60% full-scale  
+3.3V = Fan is at 75% full-scale



GND = Fan is OFF  
OPEN = Fan is at 60% full-scale  
+3.3V = Fan is at 75% full-scale

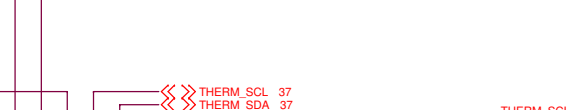


GND = Fan is OFF  
OPEN = Fan is at 60% full-scale  
+3.3V = Fan is at 75% full-scale



GND = Fan is OFF  
OPEN = Fan is at 60% full-scale  
+3.3V = Fan is at 75% full-scale

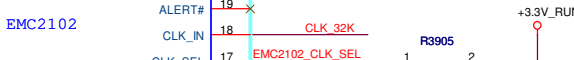
EMC2102\_FAN\_TACH <<< EMC2102\_FAN\_TACH 58  
EMC2102\_FAN\_DRIVE >>> EMC2102\_FAN\_DRIVE 58



GND = Internal Oscillator Selected  
+3.3V = External 32.768kHz Clock Selected



GND = Internal Oscillator Selected  
+3.3V = External 32.768kHz Clock Selected



GND = Internal Oscillator Selected  
+3.3V = External 32.768kHz Clock Selected



GND = Internal Oscillator Selected  
+3.3V = External 32.768kHz Clock Selected



GND = Internal Oscillator Selected  
+3.3V = External 32.768kHz Clock Selected



GND = Internal Oscillator Selected  
+3.3V = External 32.768kHz Clock Selected



GND = Internal Oscillator Selected  
+3.3V = External 32.768kHz Clock Selected



GND = Internal Oscillator Selected  
+3.3V = External 32.768kHz Clock Selected



GND = Internal Oscillator Selected  
+3.3V = External 32.768kHz Clock Selected



GND = Internal Oscillator Selected  
+3.3V = External 32.768kHz Clock Selected



Main G7922R61U for GMT P/N:74.07922.0B3  
SEC. EMC2102 for SMSC P/N:74.02102.A73

84.2N702.D31

84.2N702.D31

84.2N702.D31

84.2N702.D31

84.2N702.D31

84.2N702.D31

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84.2N702.D31

84.2N702.D31

84.2N702.D31

84.2N702.D31

CFD-20100618

CFD-20100618

CFD-20100618

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CFD-20100618

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title <b>Thermal/Fan Controllor EMC2102</b>			
Size	Document Number	Rev	X00
Custom	<b>Berry</b>		
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<Core Design>



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<Core Design>



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<Core Design>



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Title

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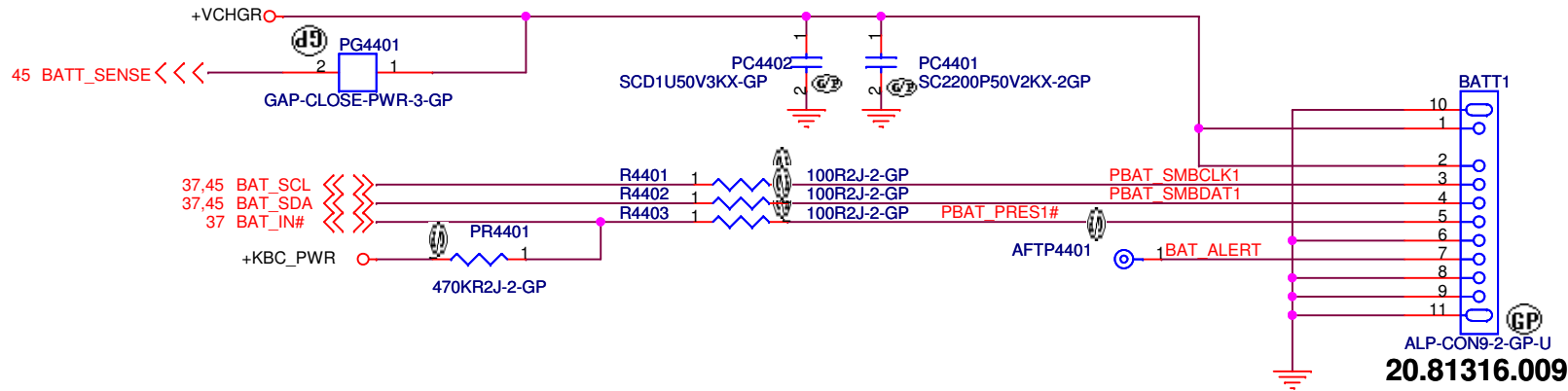
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Document Number  
Berry

Rev  
X00

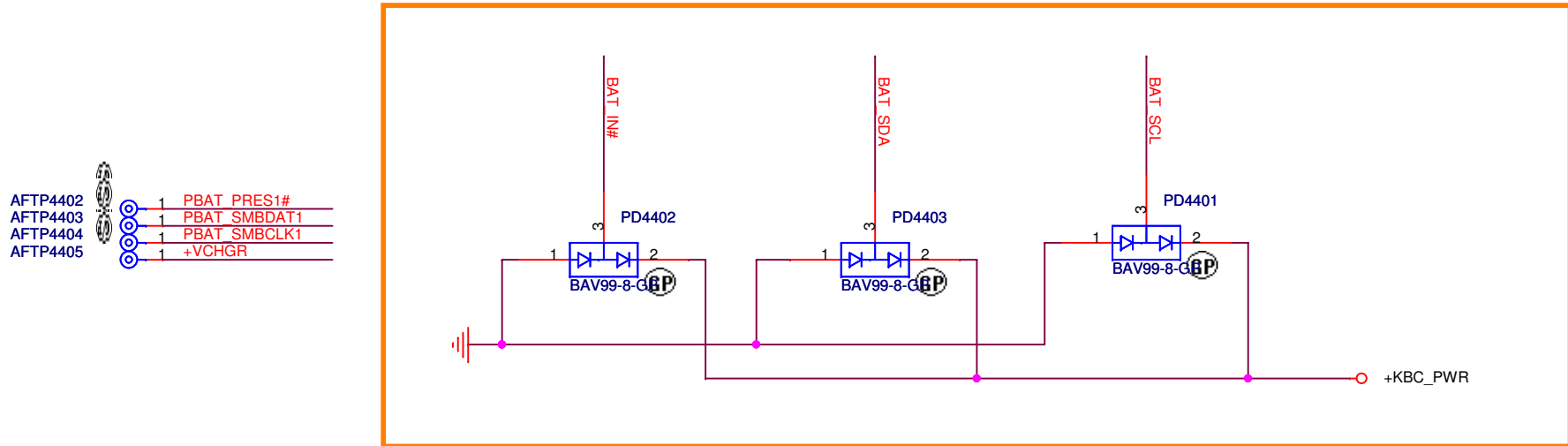
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# Batt Connector



For actual location, need to be swap all pin

## Close to Batt Connector



<Core Design>



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Title

**BATT CONN**

Size  
A4

Document Number

**Berry**

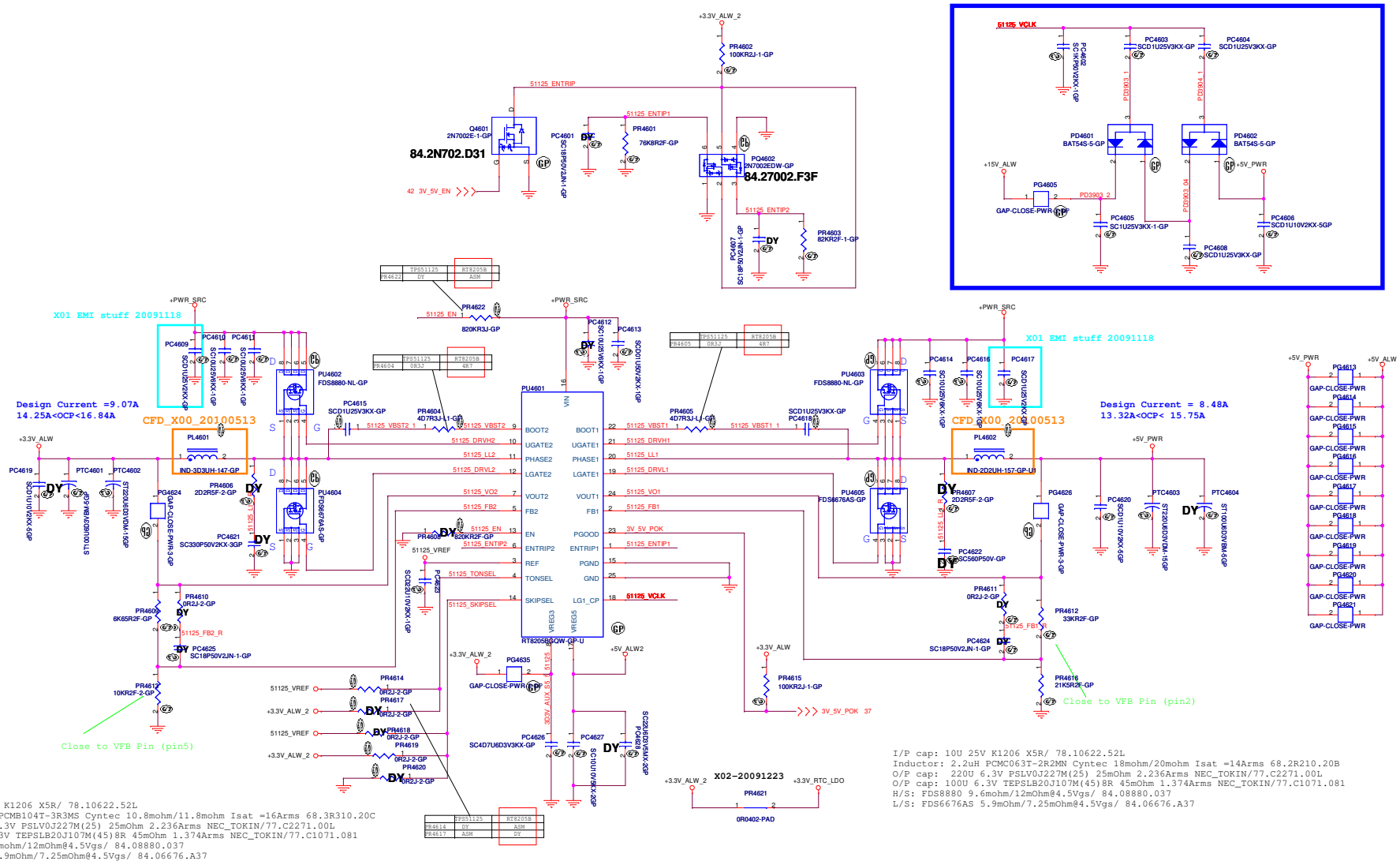
Rev

**X00**

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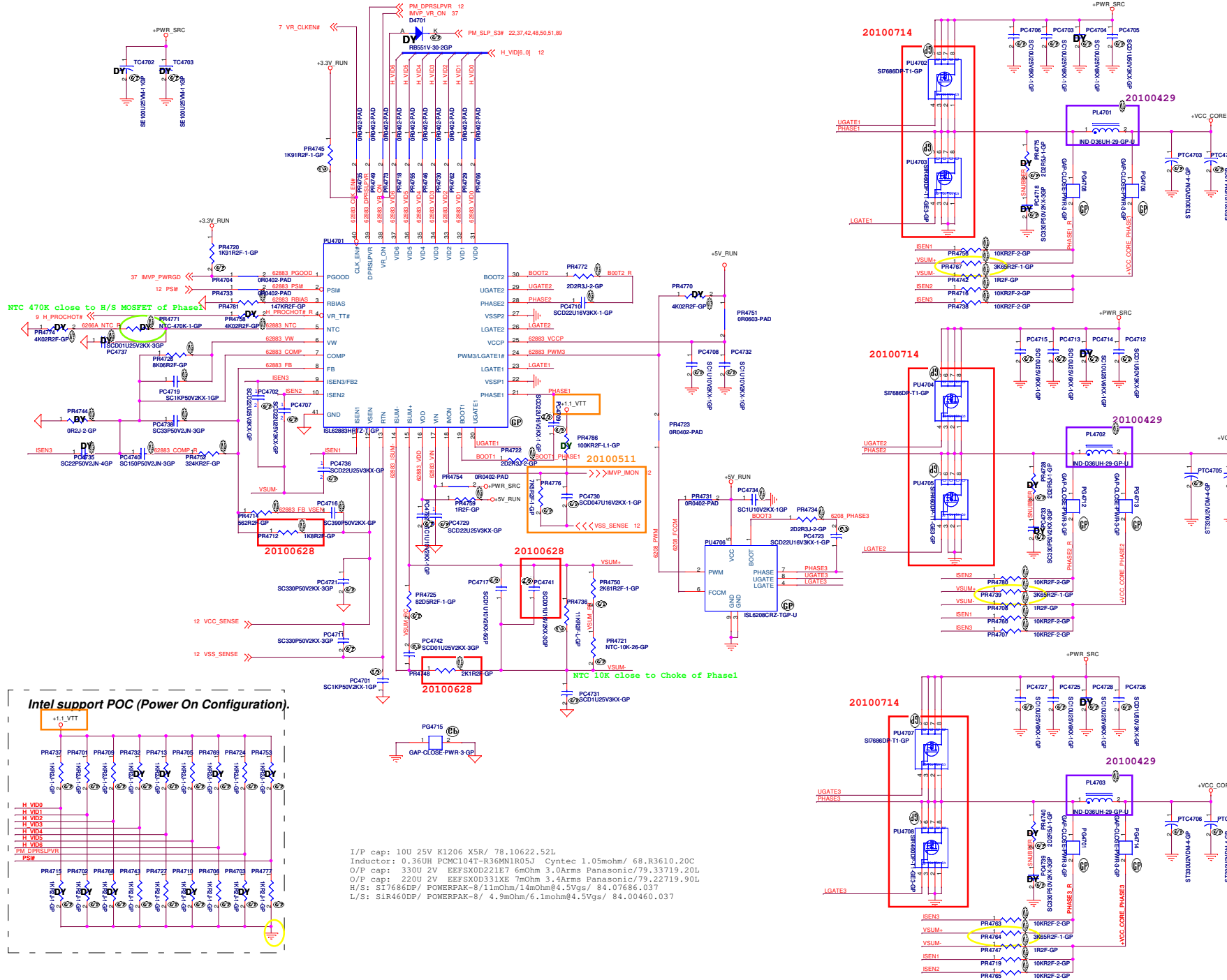
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 3.30H PCMB104T-3R3MS Cyntec 10.8mohm/11.8mohm Isat ~16Arms 68.3R310.20C  
O/P cap: 220U 6.3V PSLV0J227M(25) 25mohm 2.236Arms NEC\_TOKIN/77.C2271.00L  
O/P cap: 100U 6.3V TEP5LB20J107M(45) 8R 45mohm 1.374Arms NEC\_TOKIN/77.C1071.081  
H/S: FDS8880 9.6mohm/12mohm@4.5Vgs/ 84.08880.037  
L/S: FDS6676AS 5.9mohm/7.25mohm@4.5Vgs/ 84.06676.A37

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only
EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 2.2uH PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat ~14Arms 68.2R210.20B  
O/P cap: 220U 6.3V PSLV0J227M(25) 25mohm 2.236Arms NEC\_TOKIN/77.C2271.00L  
O/P cap: 100U 6.3V TEP5LB20J107M(45) 8R 45mohm 1.374Arms NEC\_TOKIN/77.C1071.081  
H/S: FDS8880 9.6mohm/12mohm@4.5Vgs/ 84.08880.037  
L/S: FDS6676AS 5.9mohm/7.25mohm@4.5Vgs/ 84.06676.A37



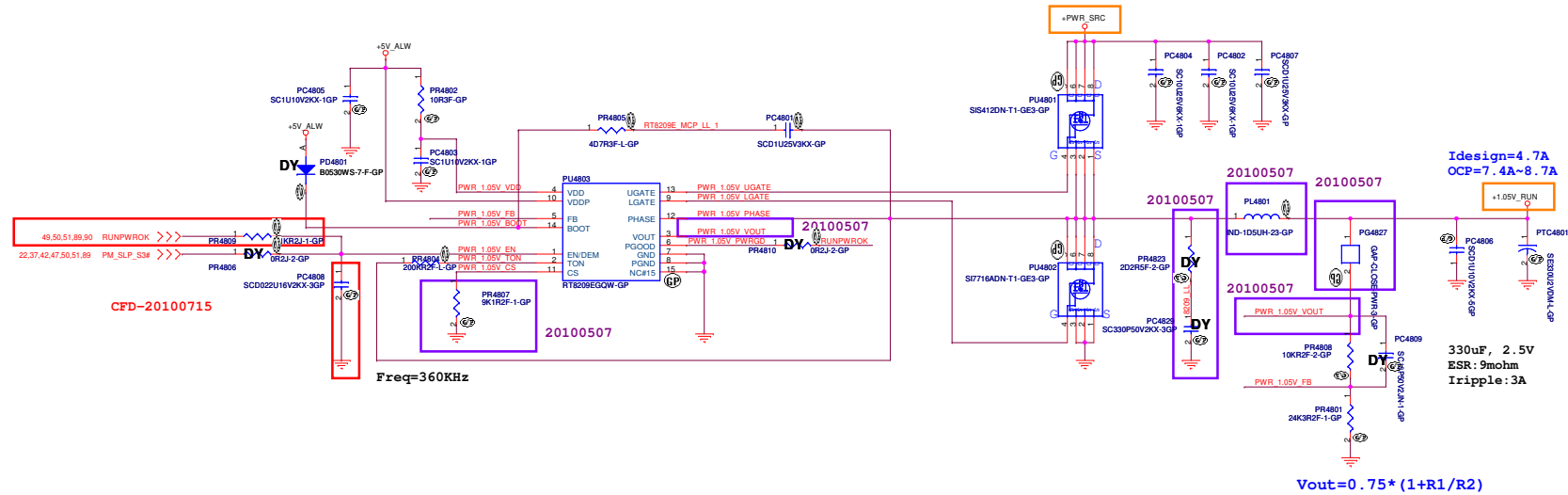
Design Current = 48A  
52.8A@OC@67.2A

Intel support POC (Power On Configuration).

I/P cap: 10U 25V K1206 XSR/ 78.10622.52L  
Inductor: 0.36uH PCM1047-R36M1R05J Cyntec 1.05mohm/ 68.R3610.20C  
O/P cap: 330U 2V EEF5X0D221E7 6mOhm 3.0Arms Panasonic/79.33719.20L  
O/P cap: 220U 2V EEF5X0D331XE 7mOhm 3.4Arms Panasonic/79.22719.90L  
H/S: SI7686DE/ POWERPAK-8/11mOhm/14mOhm/4.5Vgs/ 84.07686.037  
L/S: SI1460DE/ POWERPAK-8/ 4.9mOhm/6.1mOhm/4.5Vgs/ 84.00460.037

CFD-20100428  
Remove GAP

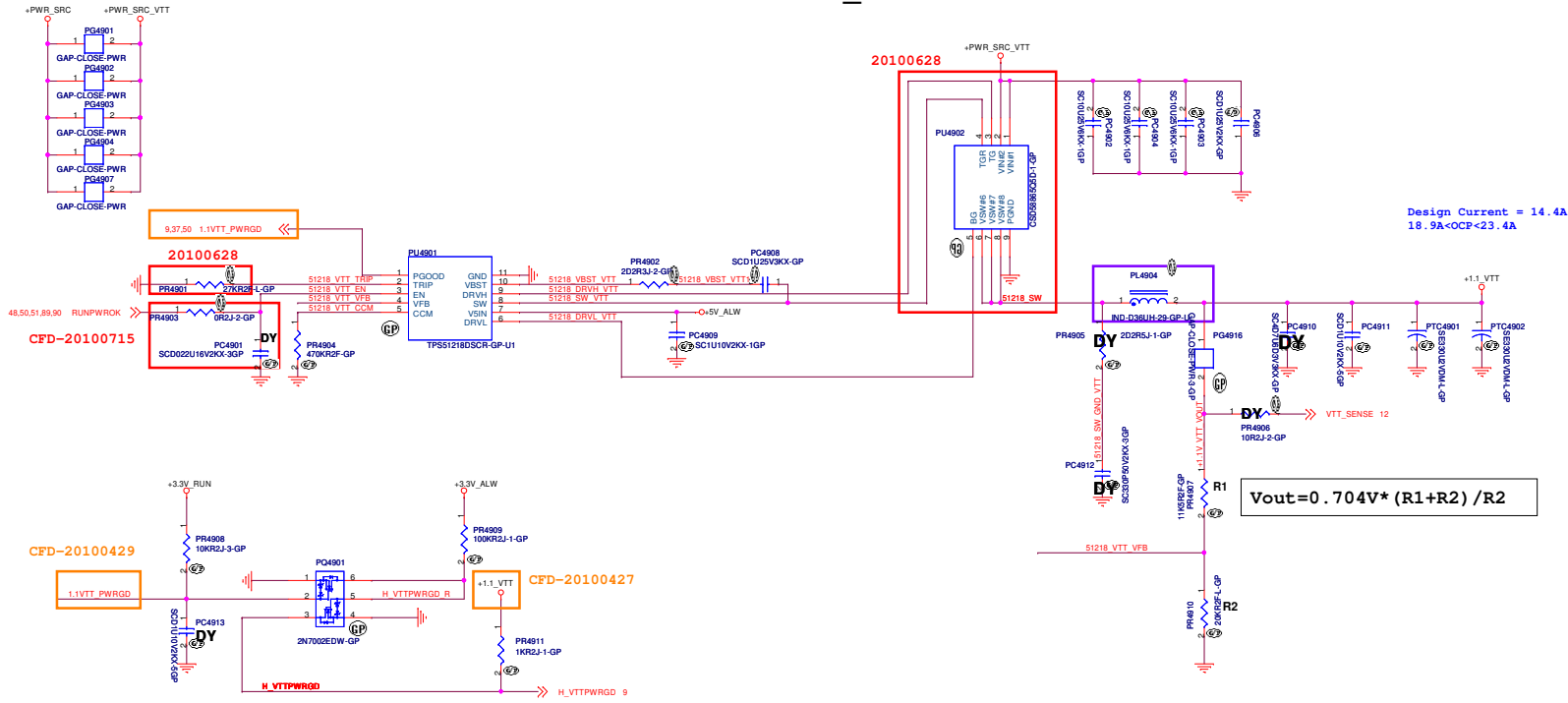
**RT8209E for +1.05V\_RUN**



CFD-20100428  
Remove GAP



# TPS51218 for +1.1V\_VTT

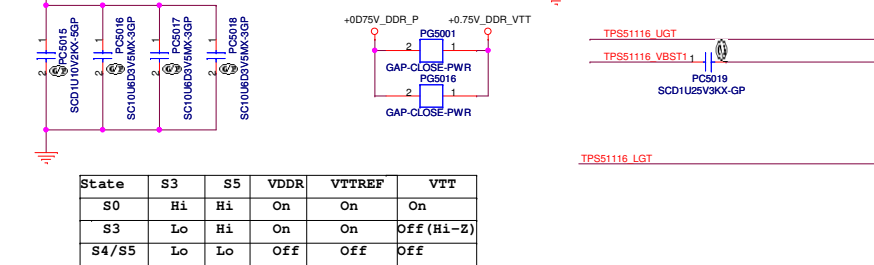


Design Current = 14.4A  
18.9A<OCP<23.4A

$$V_{out} = 0.704V * (R1 + R2) / R2$$

Frequency setting	
470K	-->290KHz
200K	-->340KHz
100K	-->380KHz
39K	-->430KHz

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 0.56uH PCMC104T-R56MN Cytec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D  
O/P cap: 330U 2.5V EEFSX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01  
H/S: S1S406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037  
L/S: S1S402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037

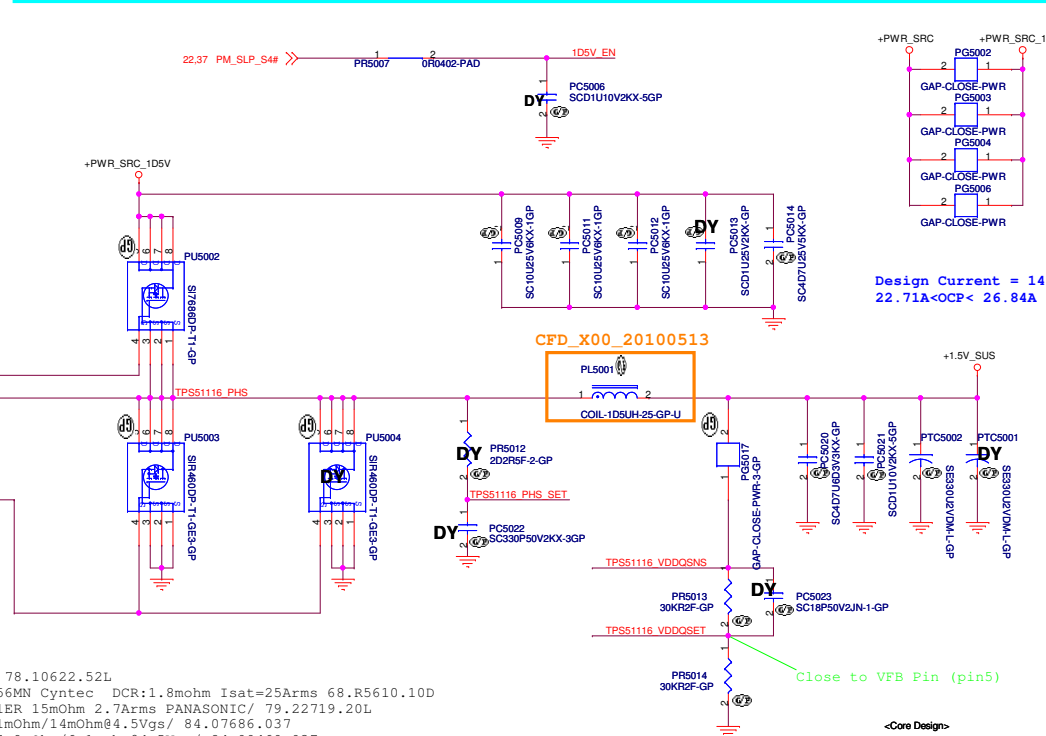
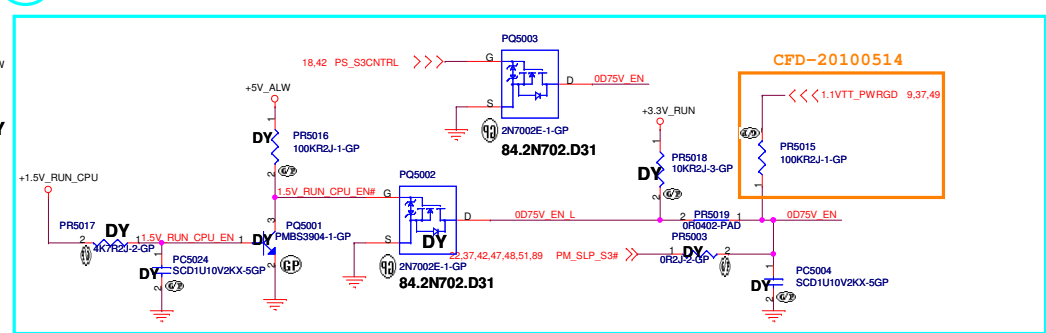


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VIT	NOTE
GND	2.5	VVDDQSNS/2	DDR
VSIN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: 0.56uH PCMC104T-R56mN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D  
O/P cap: 220U 2V EEFCX0D221ER 15mOhm 2.7Arms PANASONIC/ 79.22719.20L  
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037  
L/S: SIr460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037  
Switching freq-->400KHz

⑤ S3 Power Reduction X01 20091111



Design Current = 14.45A  
22.71A < OCP < 26.84A

Close to VFB Pin (pin5)

&lt;Core Design&gt;

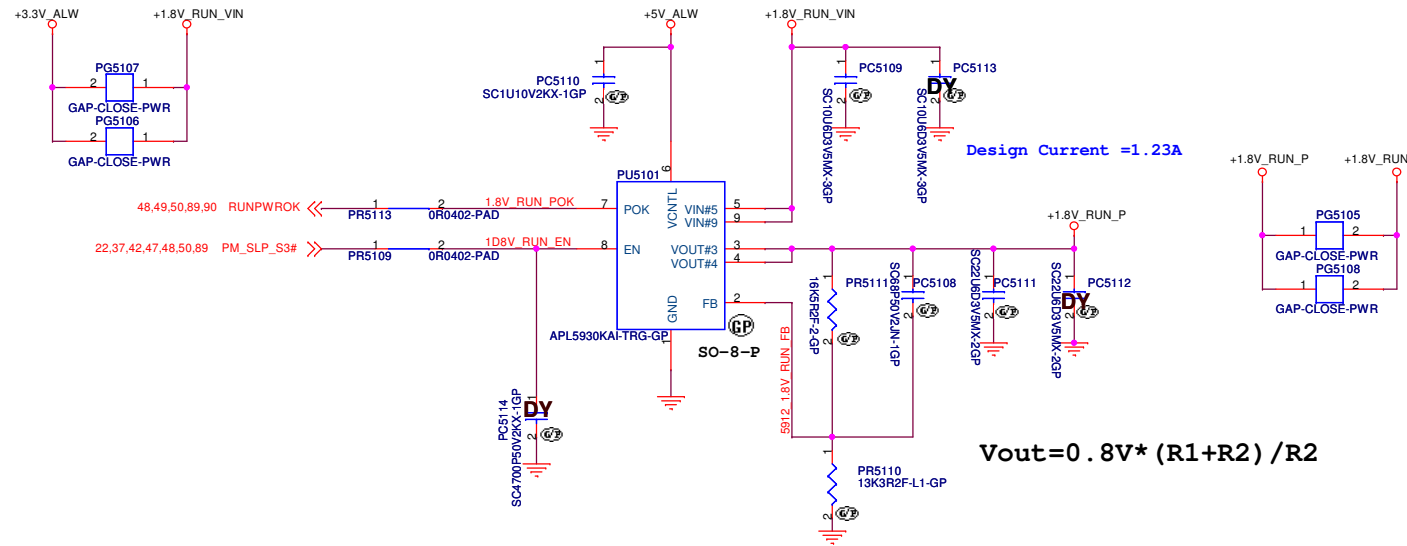


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Title			
<b>TPS51116 +1.5V SUS</b>			
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SSID = PWR.Plane.Regulator\_1p8v

## APL5930 for +1.8V\_RUN



<Core Design>



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Title

**APL5930 +1.8V\_RUN**

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A3

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<Core Design>



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Title

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```
SSID = CPU.GFX.Regulator
```

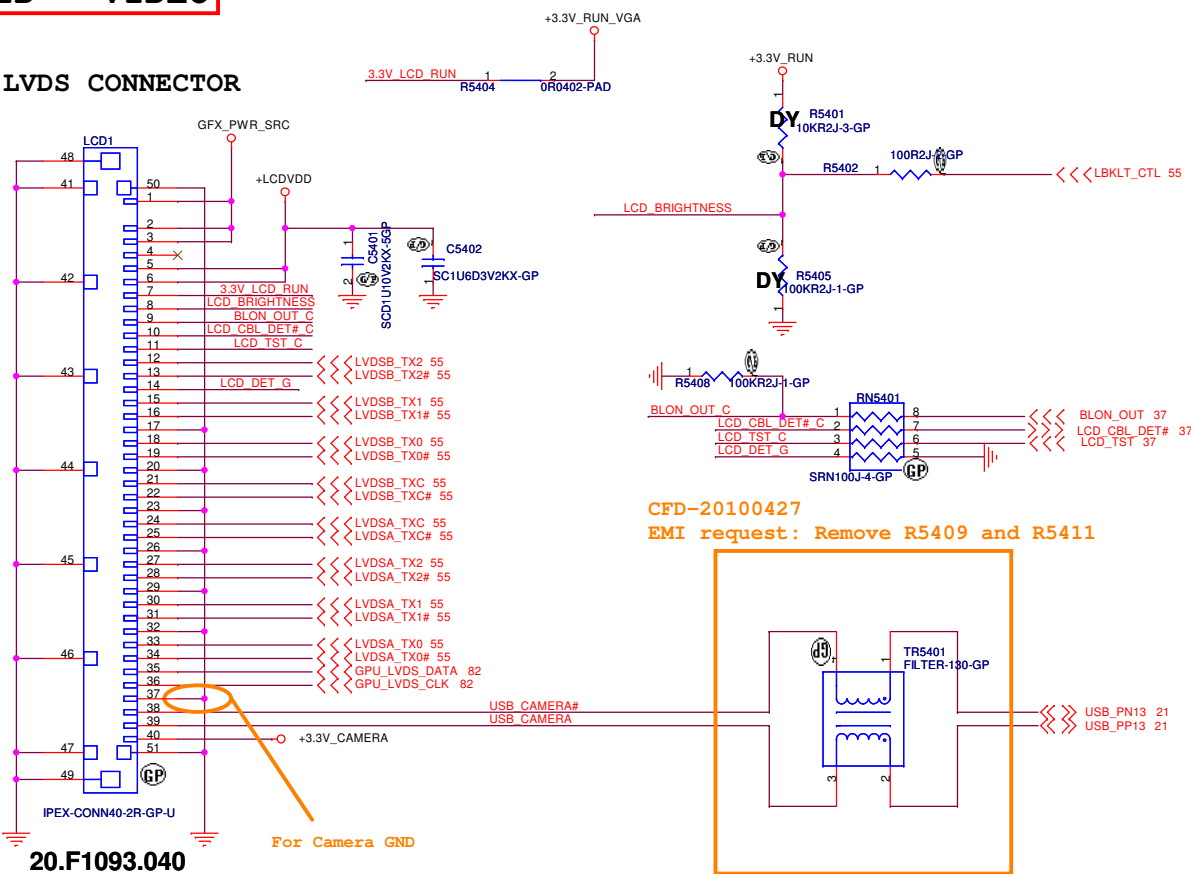
(Blanking)

CFD-20100426

Remove +GFX\_CORE

SSID = VIDEO

LVDS CONNECTOR

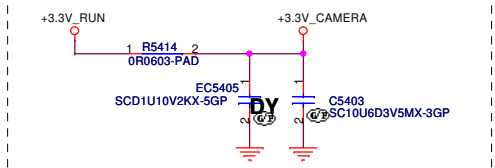


20.F1093.040

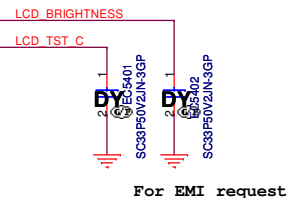
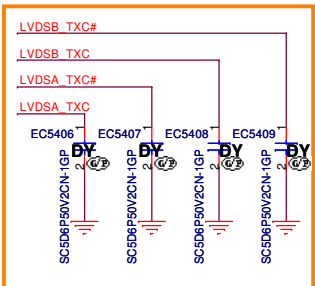
For Camera GND

CFD-20100427  
EMI request: Remove R5409 and R5411

Camera Power

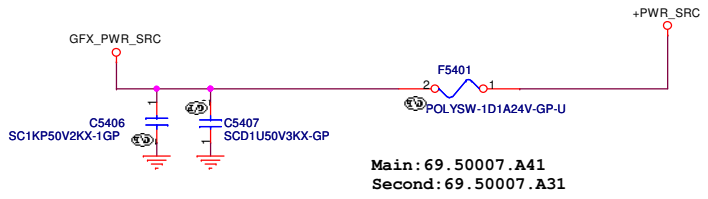


Close to LVDS connector



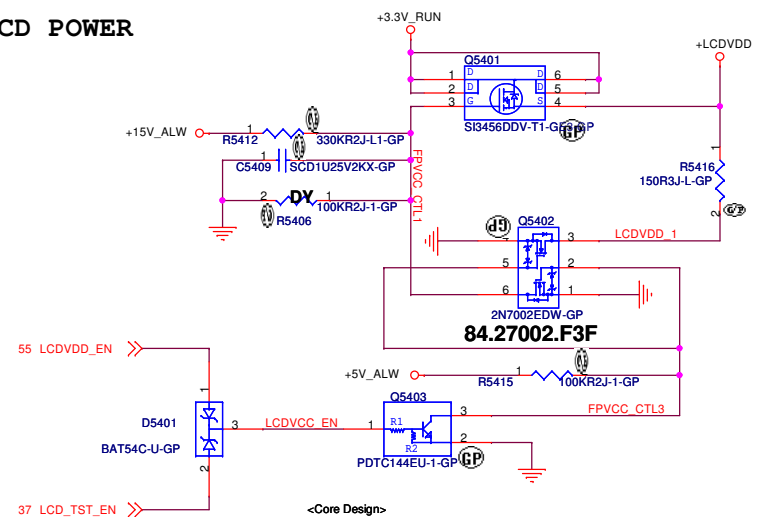
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER

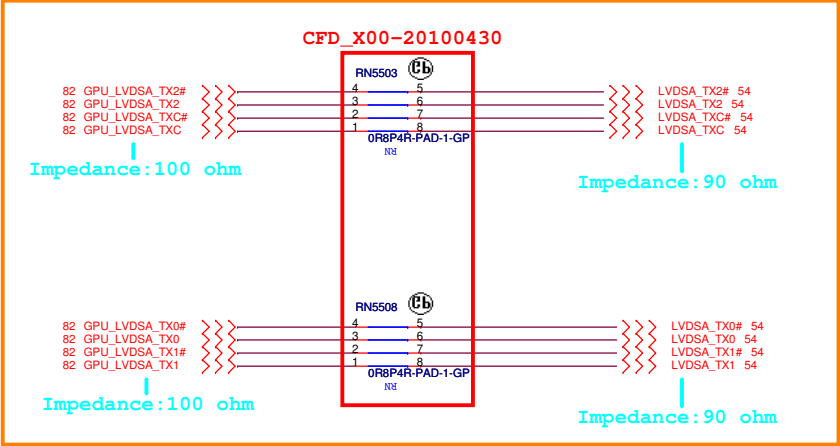


<Core Design>

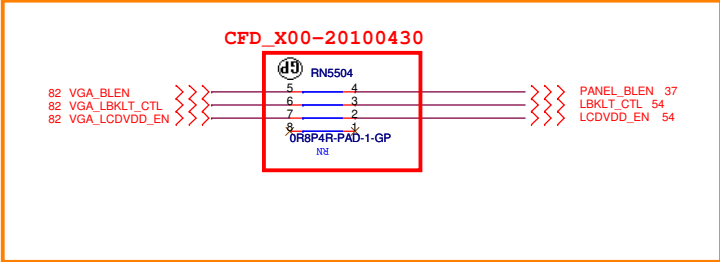
**DELL** Wistron Corporation  
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Title		LCD/Inverter Connector	
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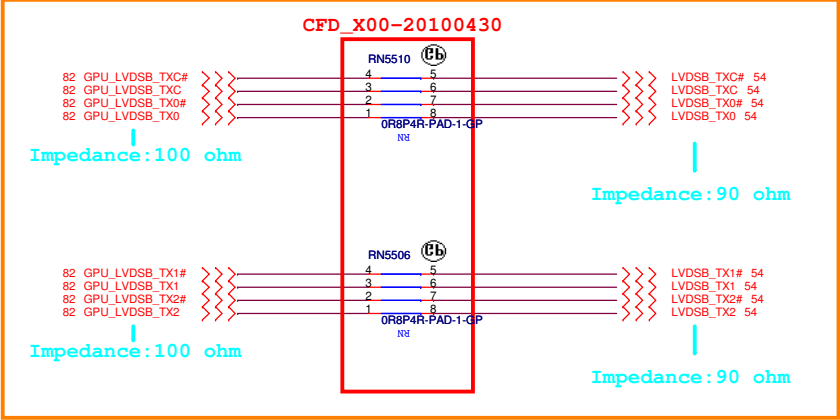
LVDS Channel A



Panel BL brightness/Power En/BL En




LVDS Channel B



(Blanking)

<Core Design>



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Title

**LVDS Switch**

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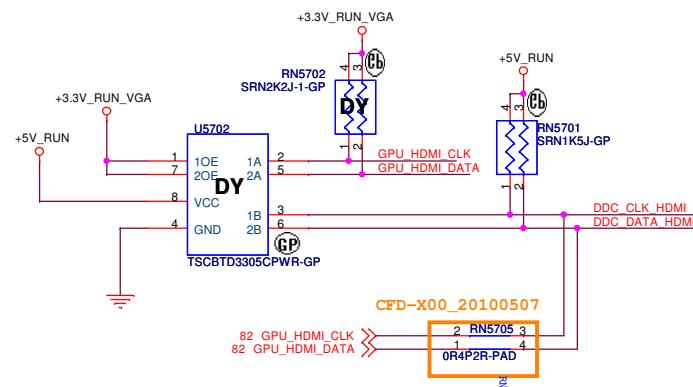
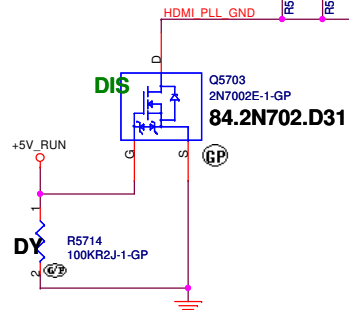
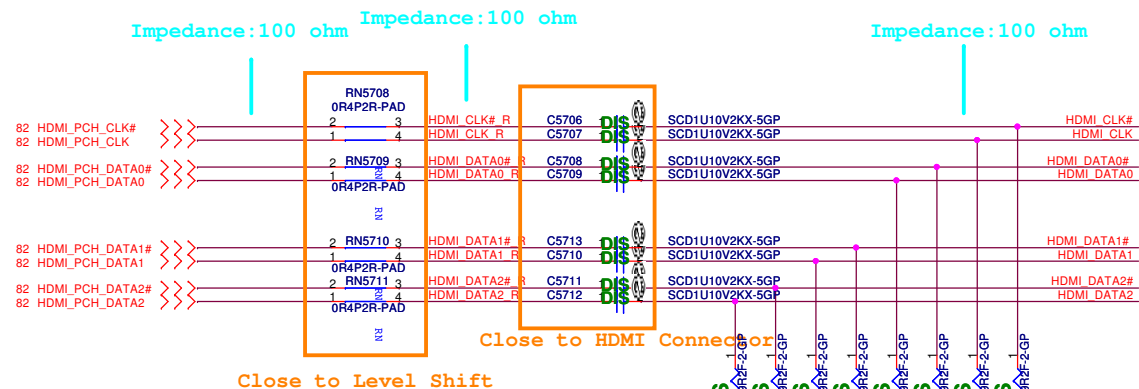
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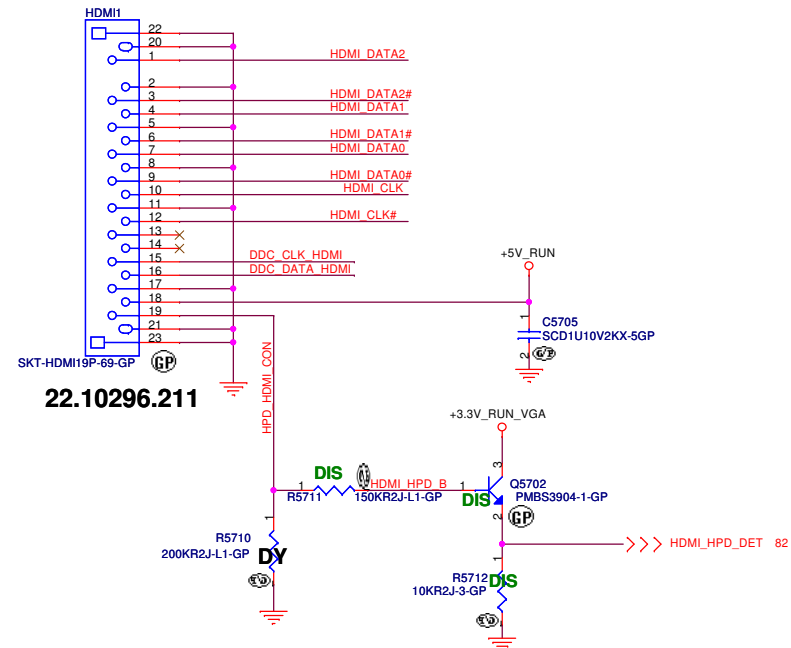
SSID = VIDEO

# HDMI CONNECTOR

HDMI DISCRETE Only



## HDMI CONN



<Core Design>

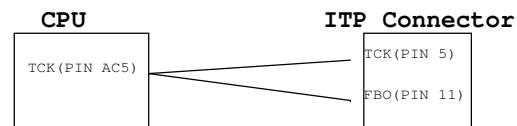
**DELL** Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

Title  
**HDMI Level Shifter/Connector**  
Size A3 Document Number **Berry** Rev **X00**  
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```
SSID = User.Interface
```

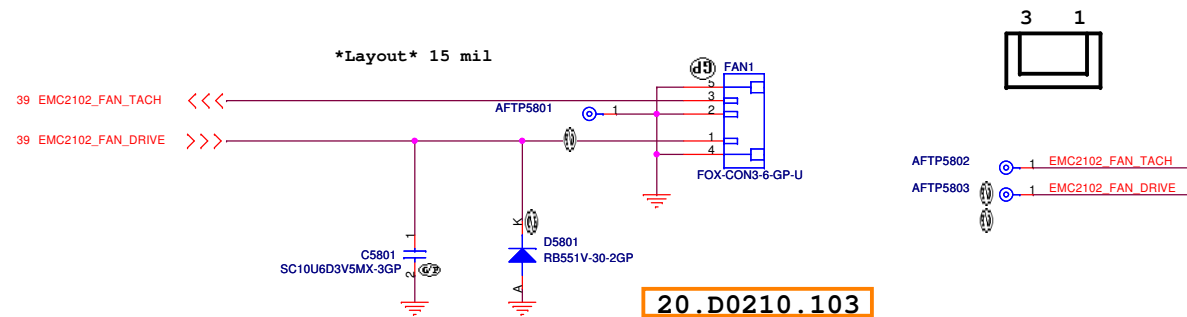
## ITP Connector

H\_CPURST# use pull-up Resistor close  
ITP connector 500 mil ( max ),  
others place near CPU side.



**SSID = Thermal**

## Fan Connector



### <Core Design>

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### **ITP/Fan Connector**

Size	A3
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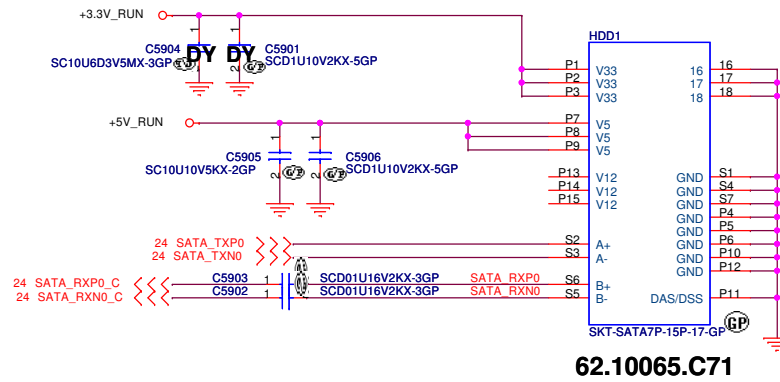
Document Number	Berny
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Rev	Y00
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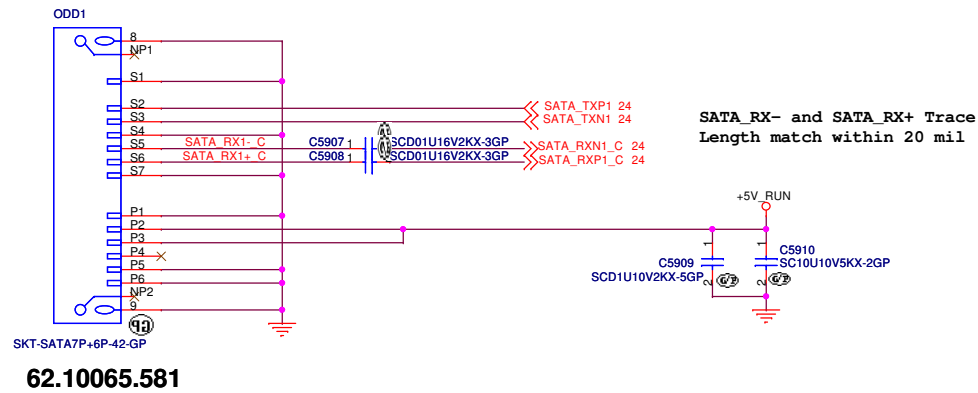
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## SATA HDD Connector



## ODD Connector



&lt;Core Design&gt;



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Title

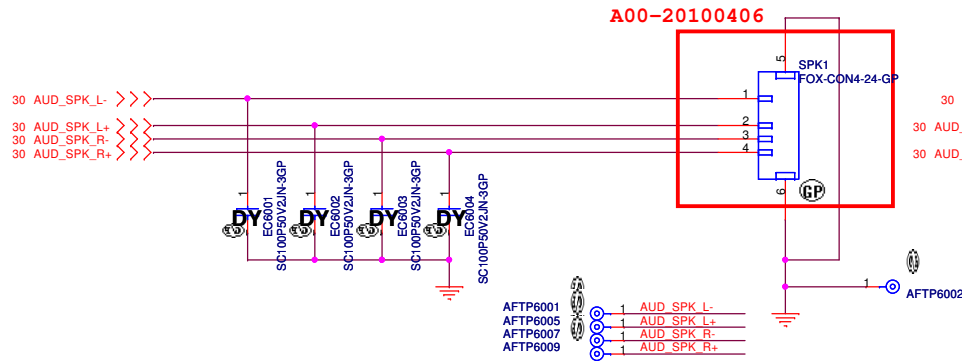
**HDD/ODD**Size  
A3Document Number  
**Berry**Rev  
**X00**

Date: Thursday, July 15, 2010

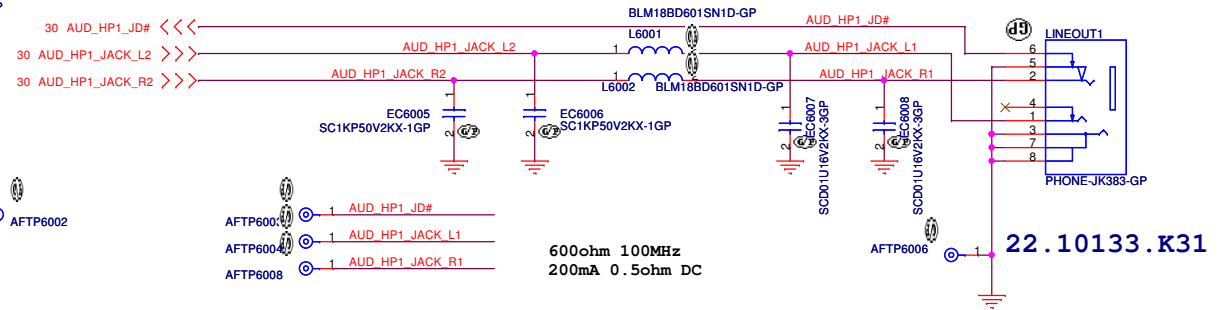
Sheet 59 of 92

SSID = AUDIO

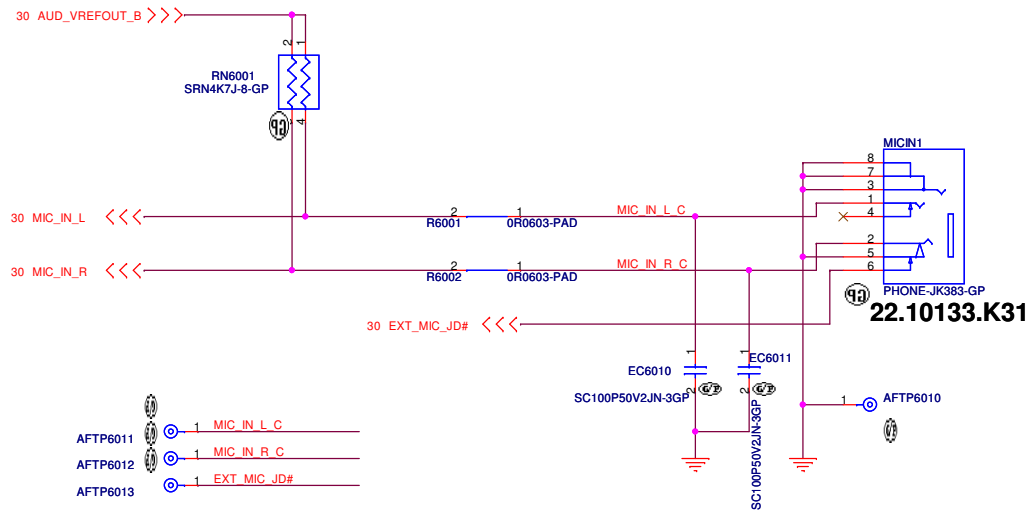
## Speaker Connector



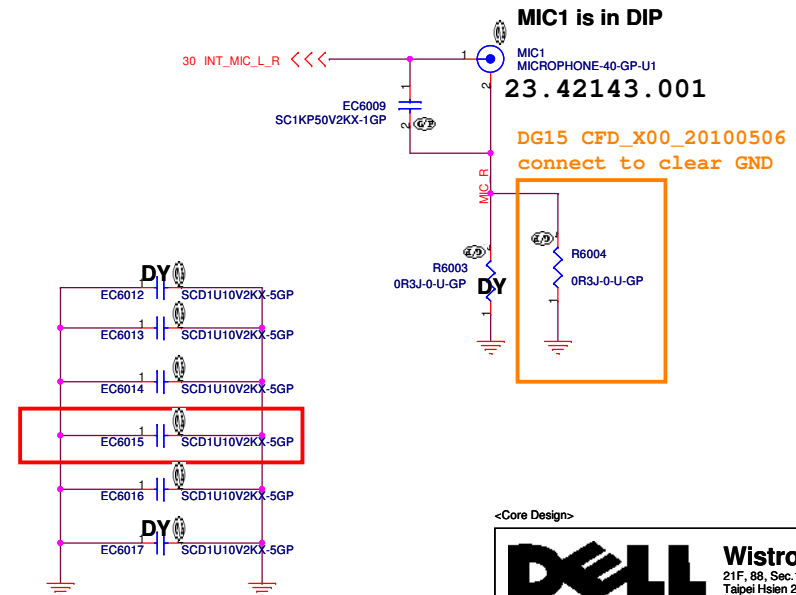
## LINE1 OUT



## MIC IN




## Internal Microphone



<Core Design>

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<Core Design>



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Title

Reserved

Size  
A3

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Berry

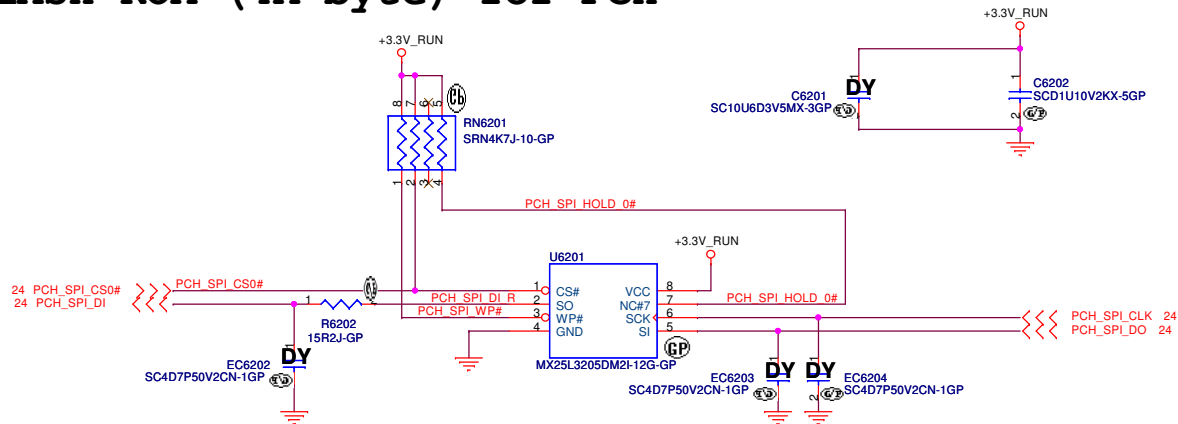
Date: Friday, May 14, 2010

Rev  
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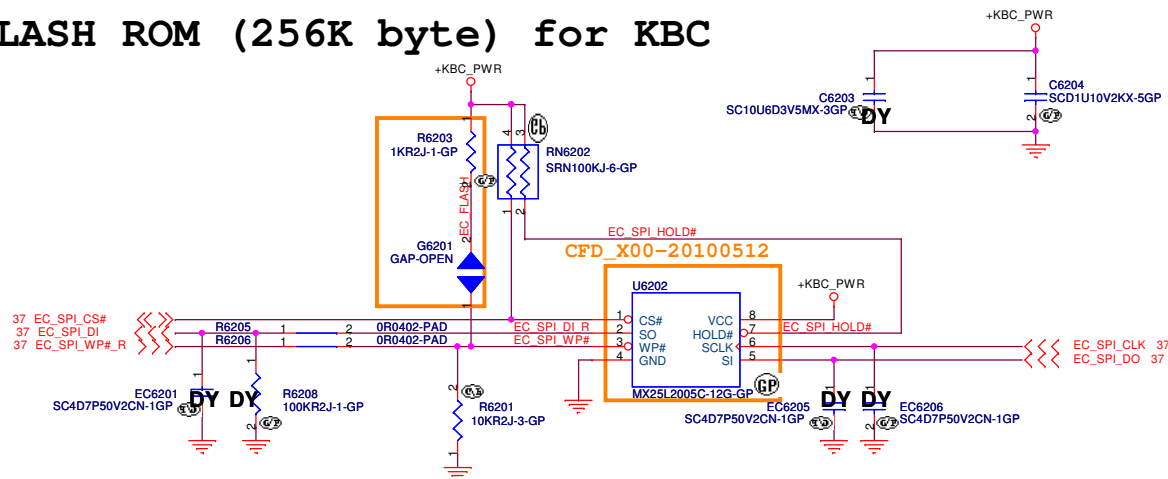
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SSID = Flash.ROM

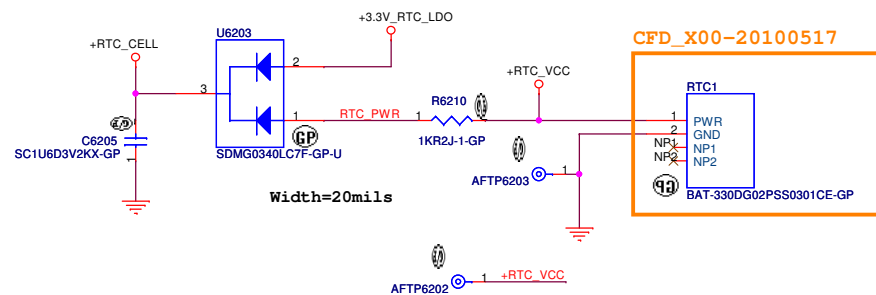
SPI FLASH ROM (4M byte) for PCH



## SPI FLASH ROM (256K byte) for KBC



**SSID = RBATT**



### <Core Design>



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Title

### ***Flash/RTC***

Size  
A3

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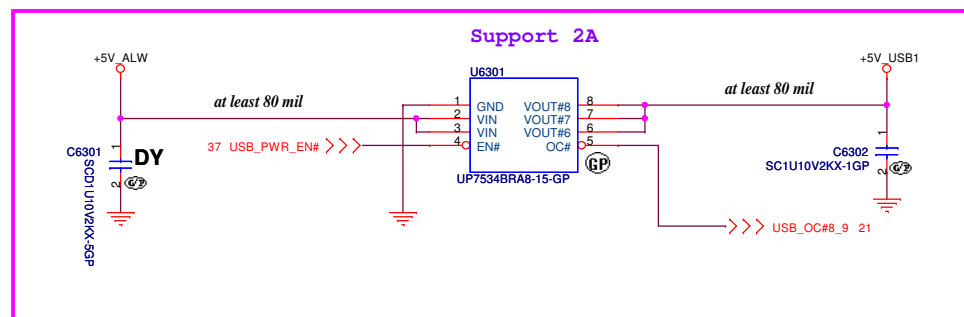
Sheet 62 of 92

**SSID = USB**

## IO Board USB Power

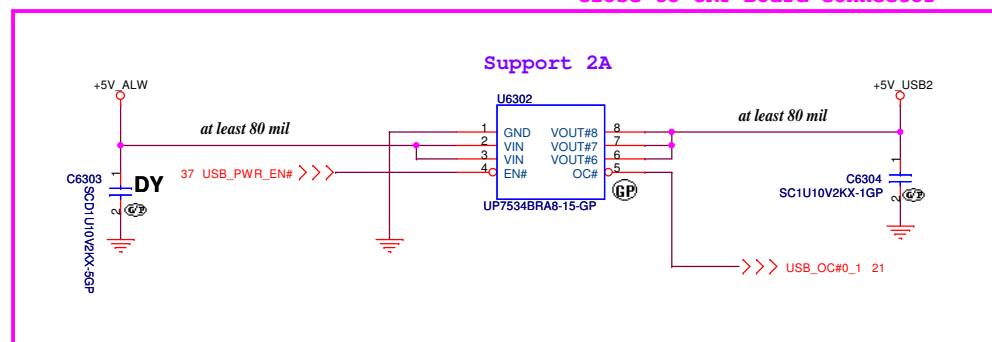
USB POWER SW  
Main UP7534BRA8-15 P/N:74.07534.079  
SEC AP2101MPG-13 P/N: 74.02101.079

Close to I/O connector



## CRT Board USB Power

Close to CRT Board connector



### <Core Design>



	Title
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### **USB Power SW**

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	<b>Ber</b>


Rev	<b>X00</b>
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<Core Design>

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Title <b>Reserved</b>			
Size A4	Document Number <b>Berry</b>		Rev <b>X00</b>
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<Core Design>



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Title

Size  
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<Core Design>



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Title

Size

A3

Document Number

**Berry**

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**X00**

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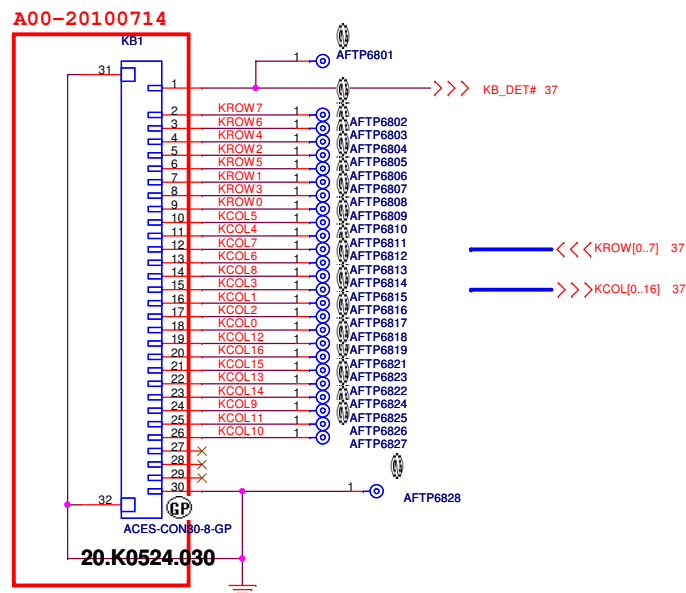
of

92

**Reserved**

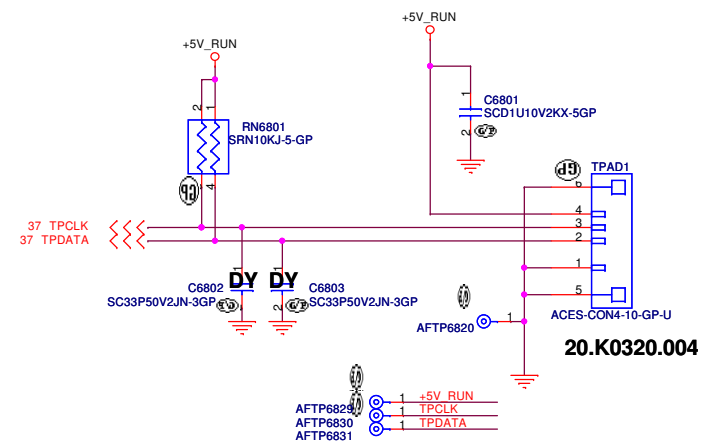
SSID = KBC

## Internal Keyboard Connector

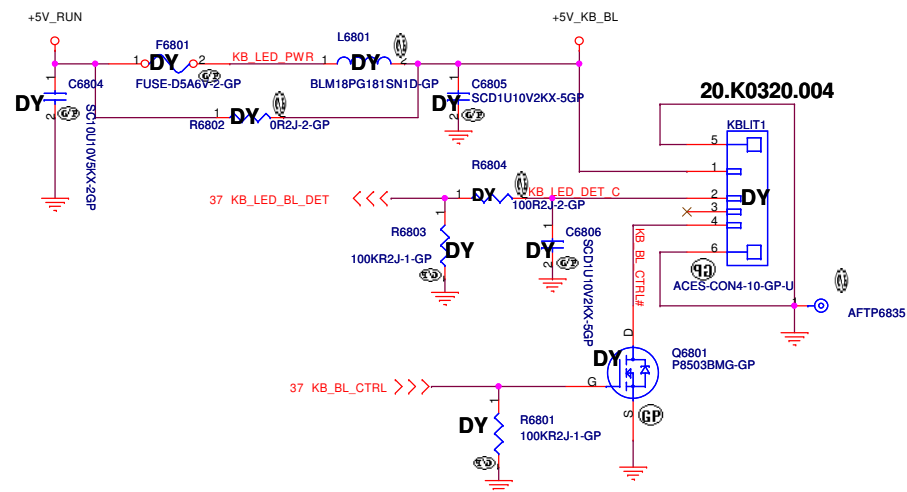


SSID = Touch.Pad

## TouchPad Connector



## KB Backlight Connector



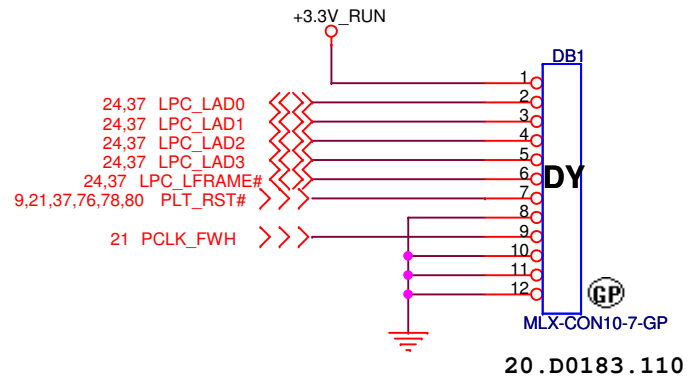
<Core Design>



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Title		Key Board/Touch Pad	
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<Core Design>



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Title

***Dubug connector***

Size  
A4

Document Number

***Berry***


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***X00***

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<Core Design>



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Title

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<Core Design>



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Title

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A3

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Rev  
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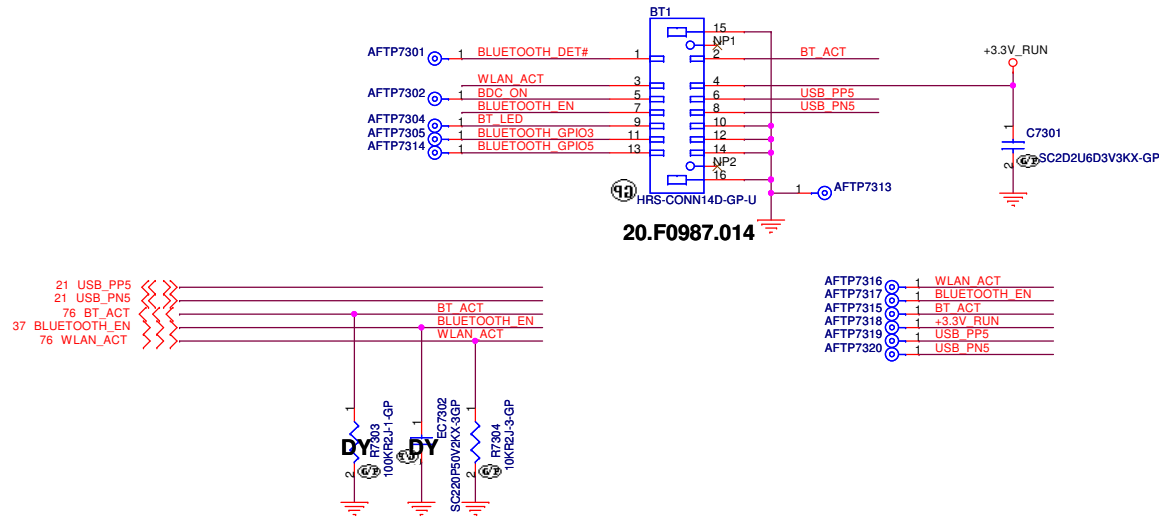
**RESERVED**

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SSID = User.Interface

## Bluetooth Module conn.



<Core Design>



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Title

**Bluetooth**

Size  
A3

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<Core Design>



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Title

Size  
A3

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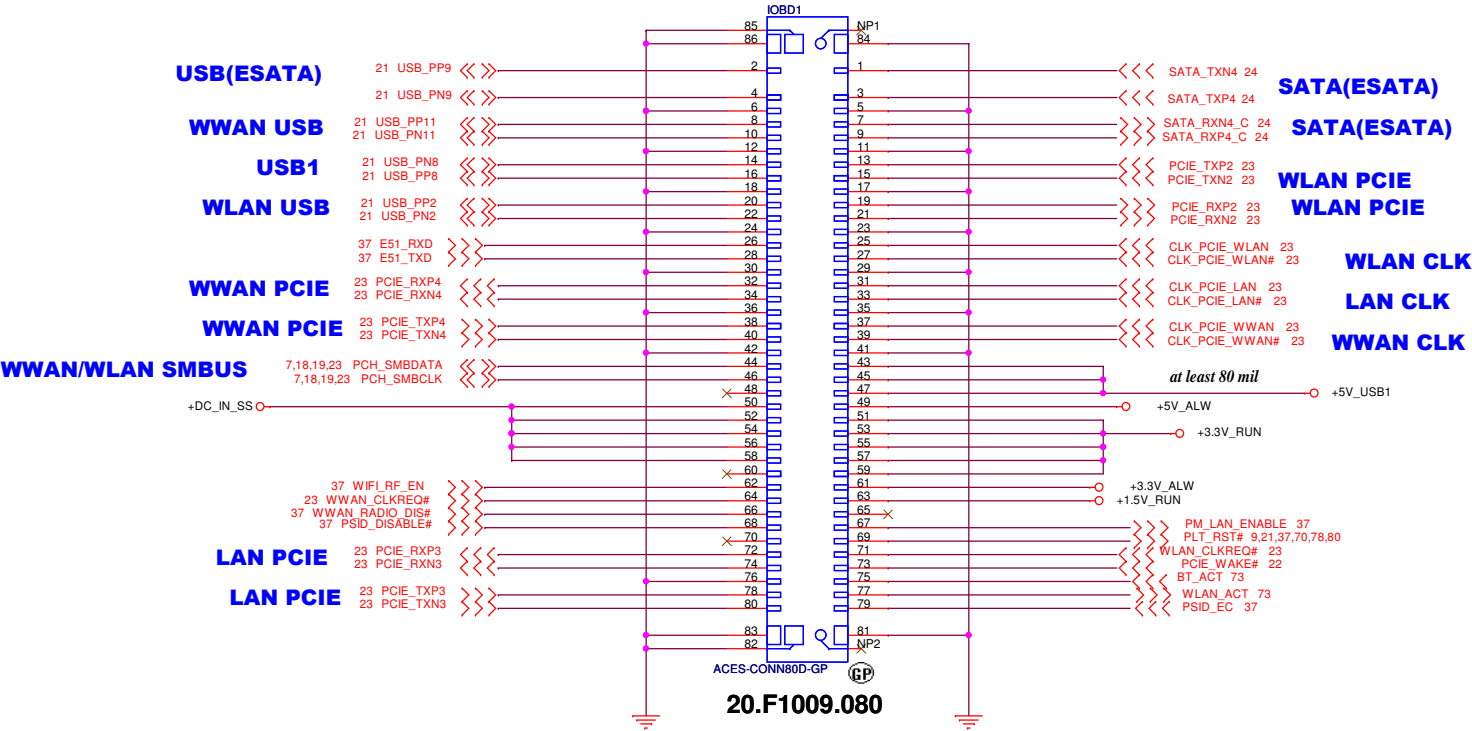
Reserved

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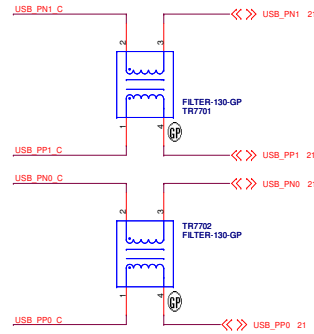
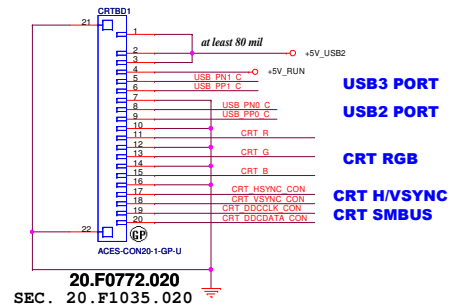
<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Reserved</b>			
Size A4	Document Number <b>Berry</b>		Rev <b>X00</b>
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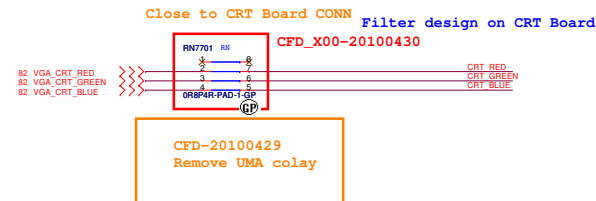
IO Board CONN 80 pin



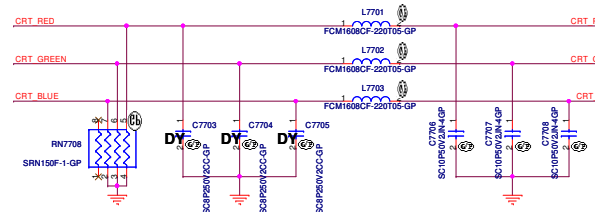
## CRT Board Connector



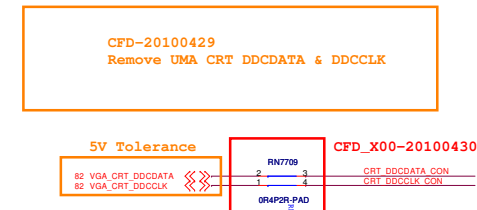
### CRT RGB



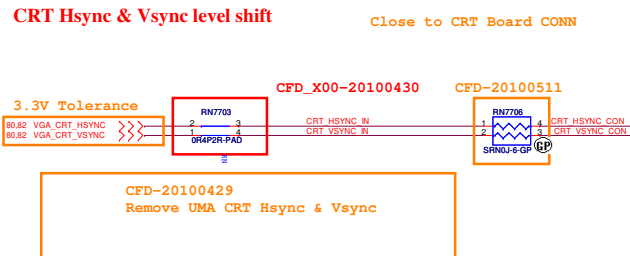
### CRT RGB



### CRT DDCDATA & DDCLK level shift



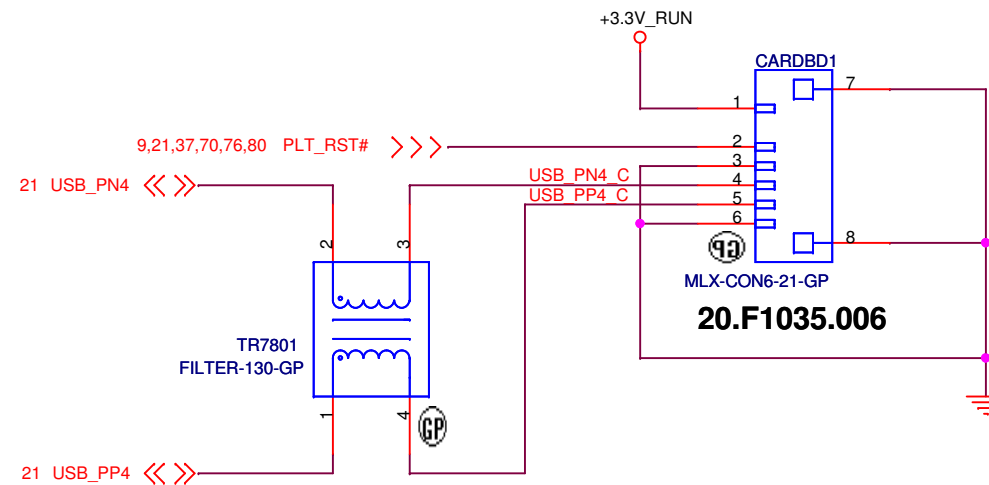
### CRT Hsync & Vsync level shift



<Core Design>

SSID = SDIO

## Card Reader connector



<Core Design>



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Title

**CARD Reader CONN**

Size  
A4

Document Number

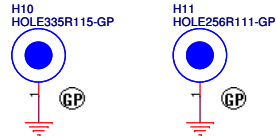
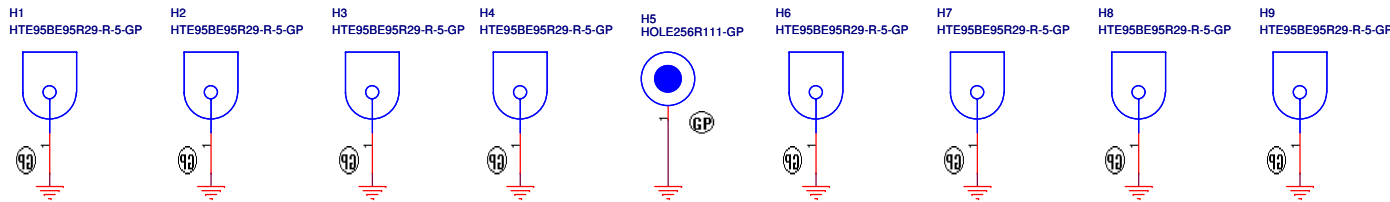
**Berry**

Rev

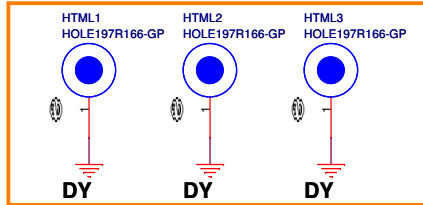
**X00**

Date: Thursday, July 15, 2010

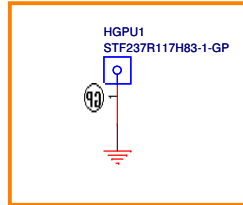
Sheet 78 of 92



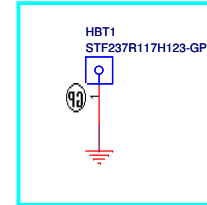
CPU Thermal module hole



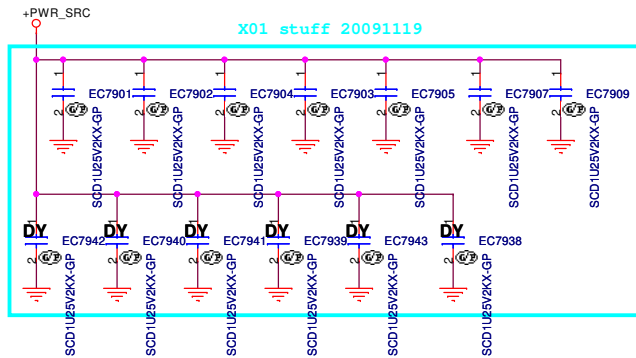
GPU Thermal module hole



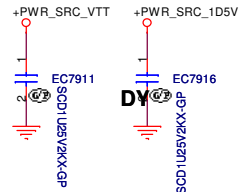
stand off



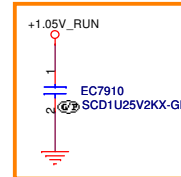
## EMI Reserve



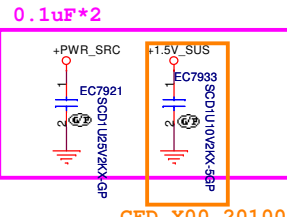
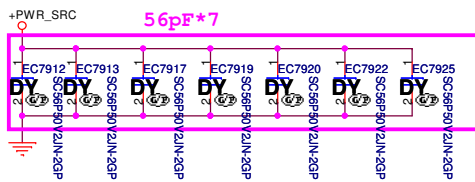
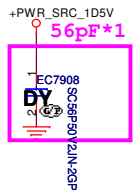
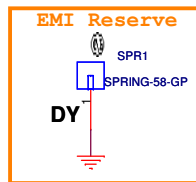
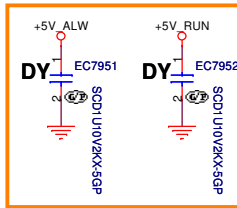
CFD-20100427  
Remove +VGFXCORE\_PWR\_SRC



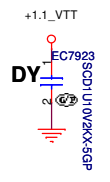
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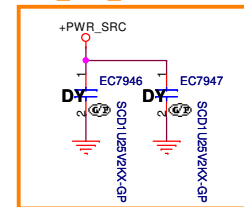
CFD\_X00\_20100514



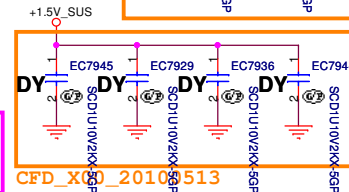
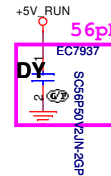
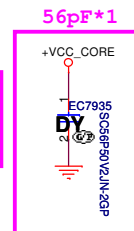
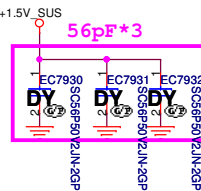
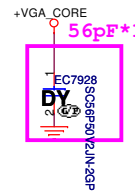
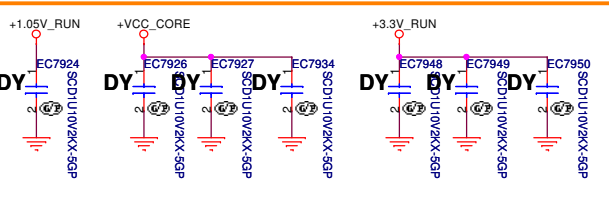
CFD\_X00\_20100513



CFD\_X00\_20100513



CFD\_X00\_20100513



CFD\_X00\_20100513

<Core Design>

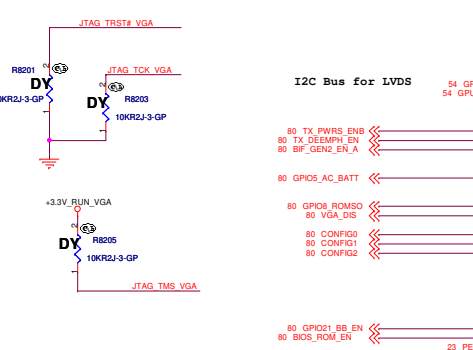




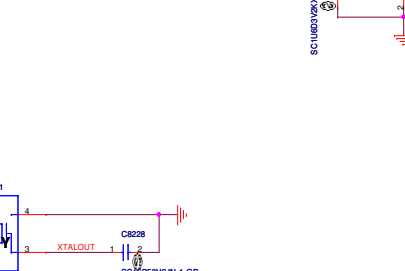
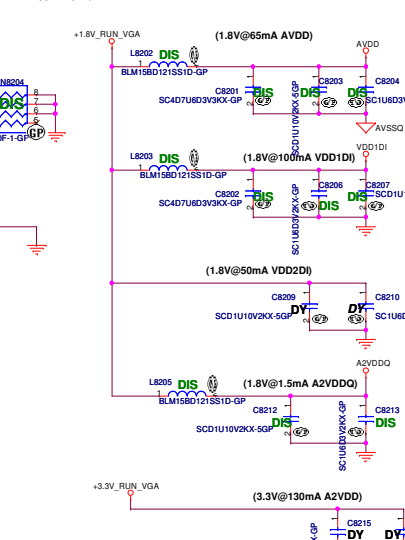
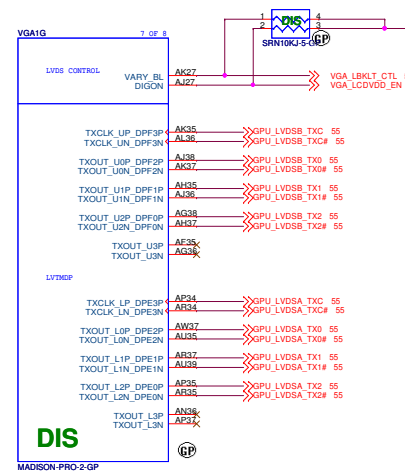
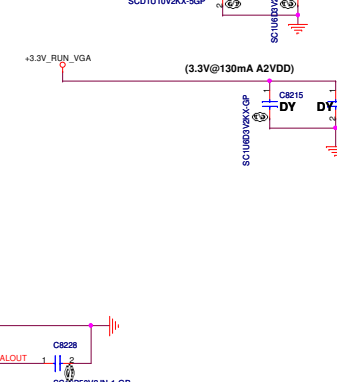
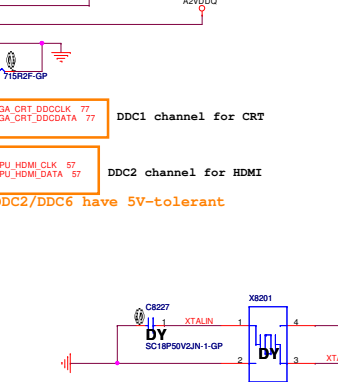
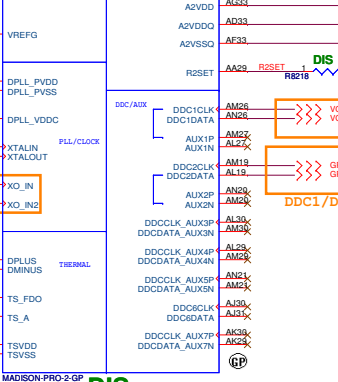
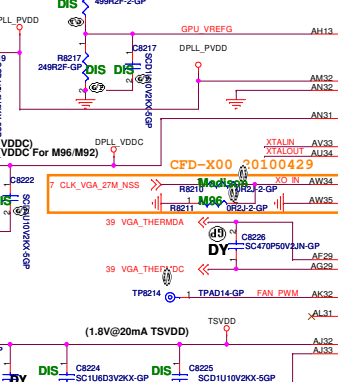


DVDPDATA[0:3]	Description
0001	DDR3 Hynix-H5TQ1G63BFR-12C (800MHz) 64M*16
0011	DDR3 Hynix-H5TQ2G63BFR-12C (800MHz) 128M*16
0010	DDR3 SAMSUNG K4W2G1646B-HC12 (800MHz) 128M*16
0000	DDR3 SAMSUNG-K4W1G1646E-HC12 (800MHz) 64M*16

DVDPDATA[0:3] Default: Pull down

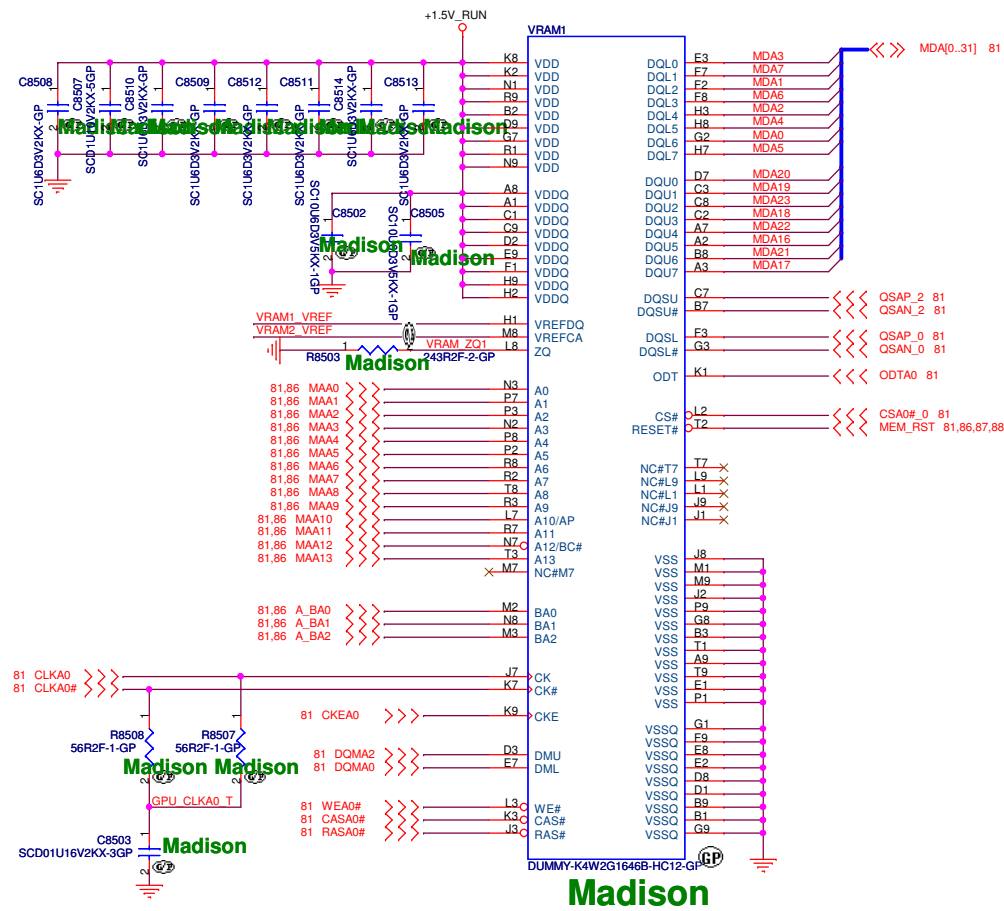


The image shows a detailed PCB layout with two main power planes. The top plane is labeled "CLOSE TO ASIC" and contains components L8001, C8205, SC4D7U8D3V3KX-GP, C8218, and C8219. It is powered by 1.8V\_RUN\_VGA and 1.0V\_RUN\_VGA. The bottom plane contains components L8007, C8220, SC4D7U8D3V3KX-GP, C8221, and C8222, also powered by 1.0V\_RUN\_VGA and 1.8V\_RUN\_VGA. A red box highlights a section of the bottom plane with labels CLK\_VGA, M96, RB212, XTALIN, and RB213. Various other labels like "DIS", "BY", and "D" are scattered throughout the layout.

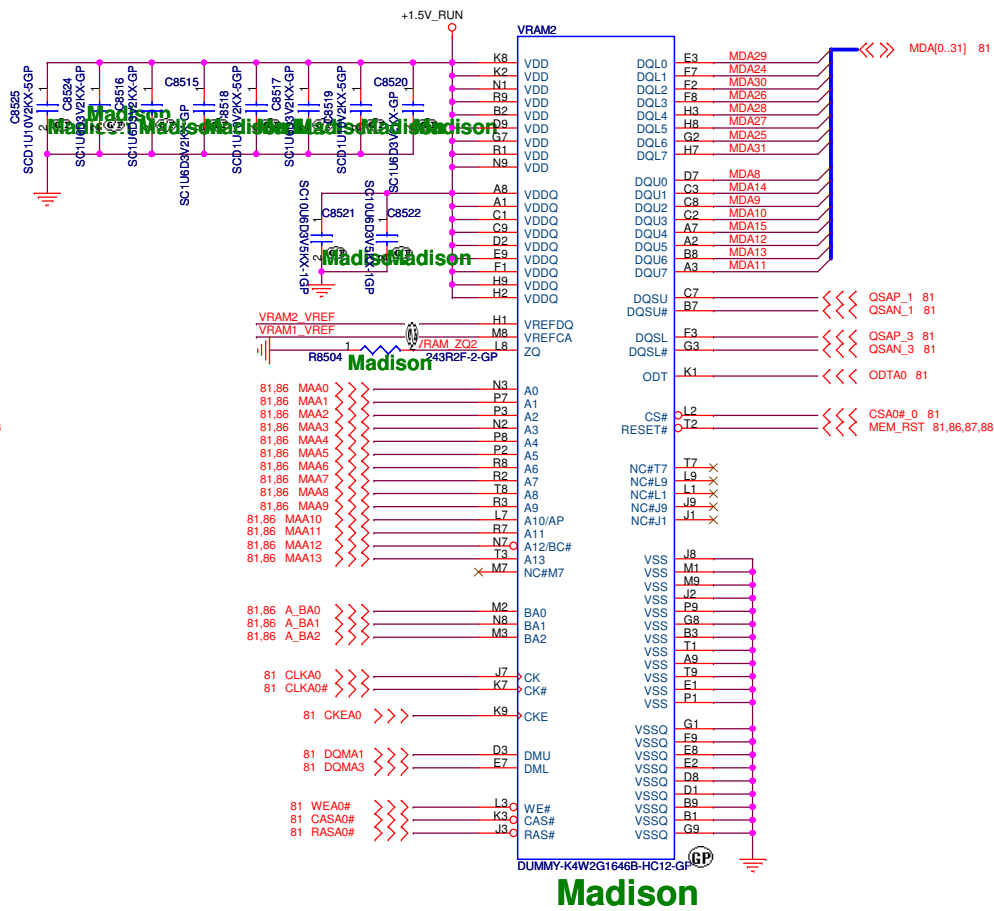




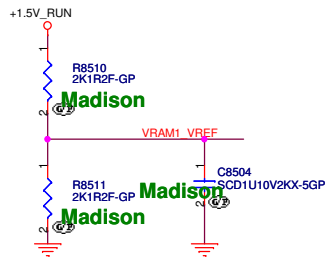




**Madison**

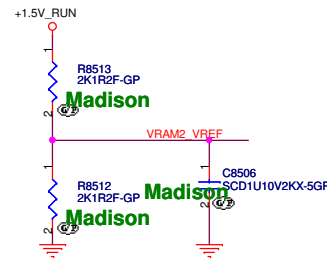


**Madison**



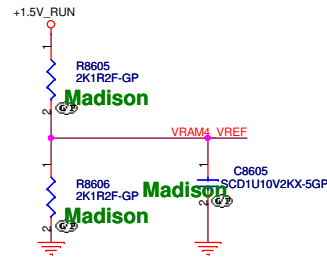
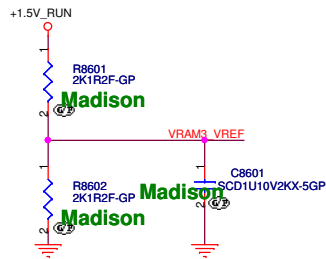
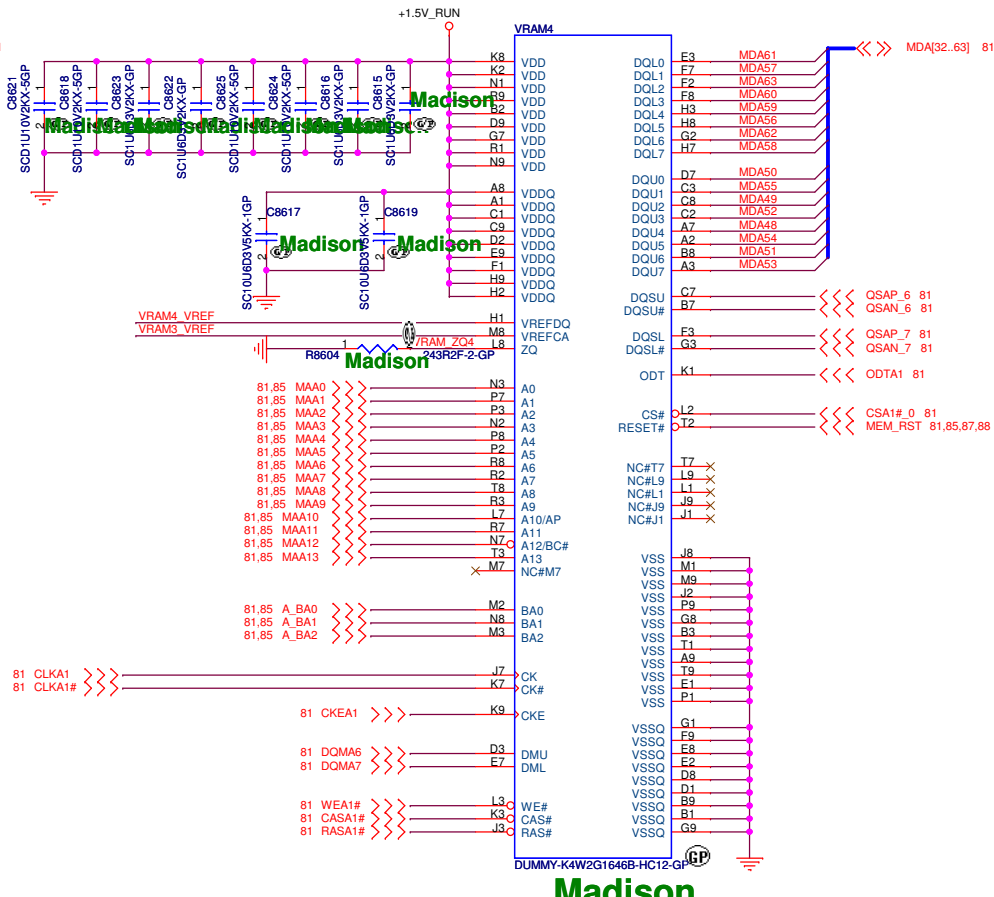
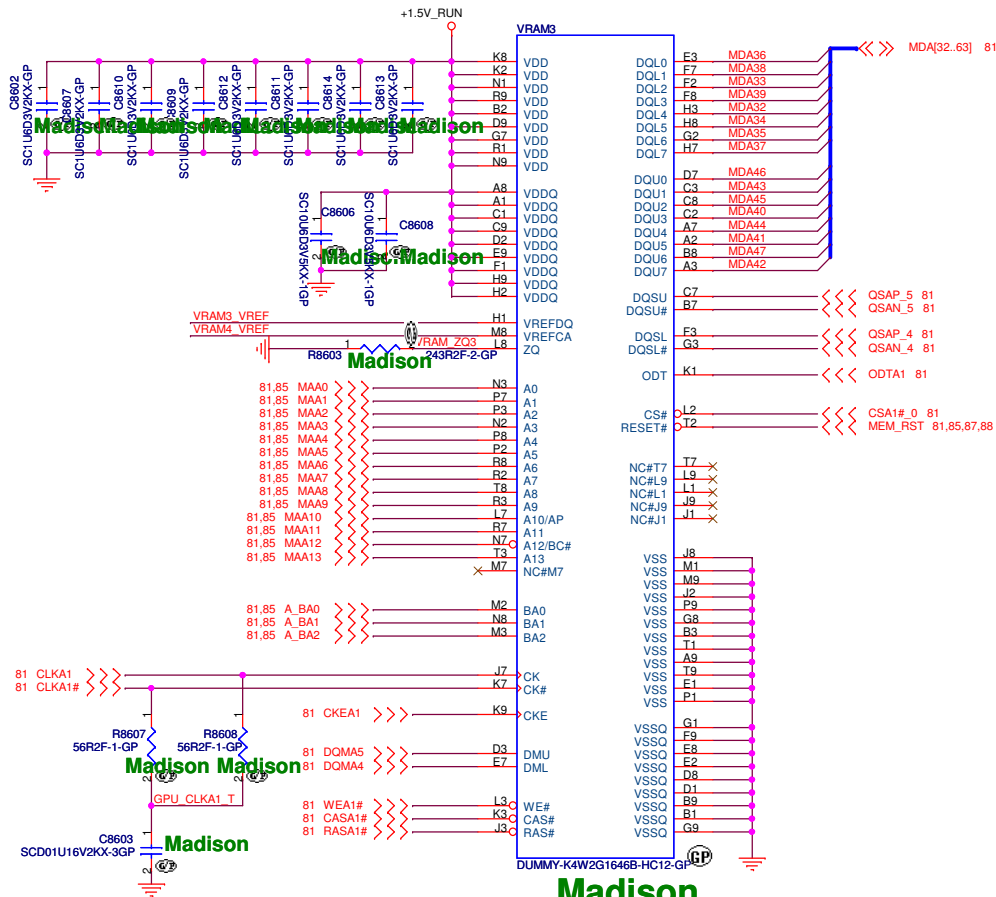
**Madison**

**Madison**



**Madison**

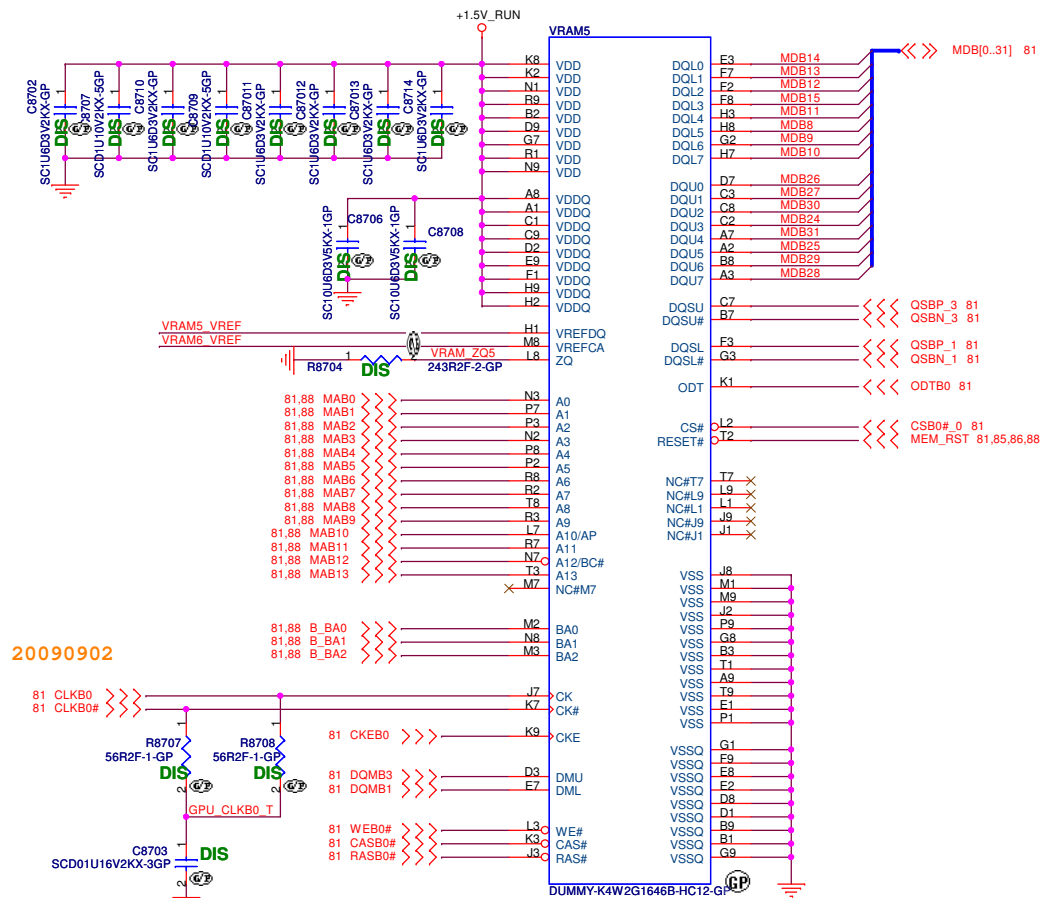
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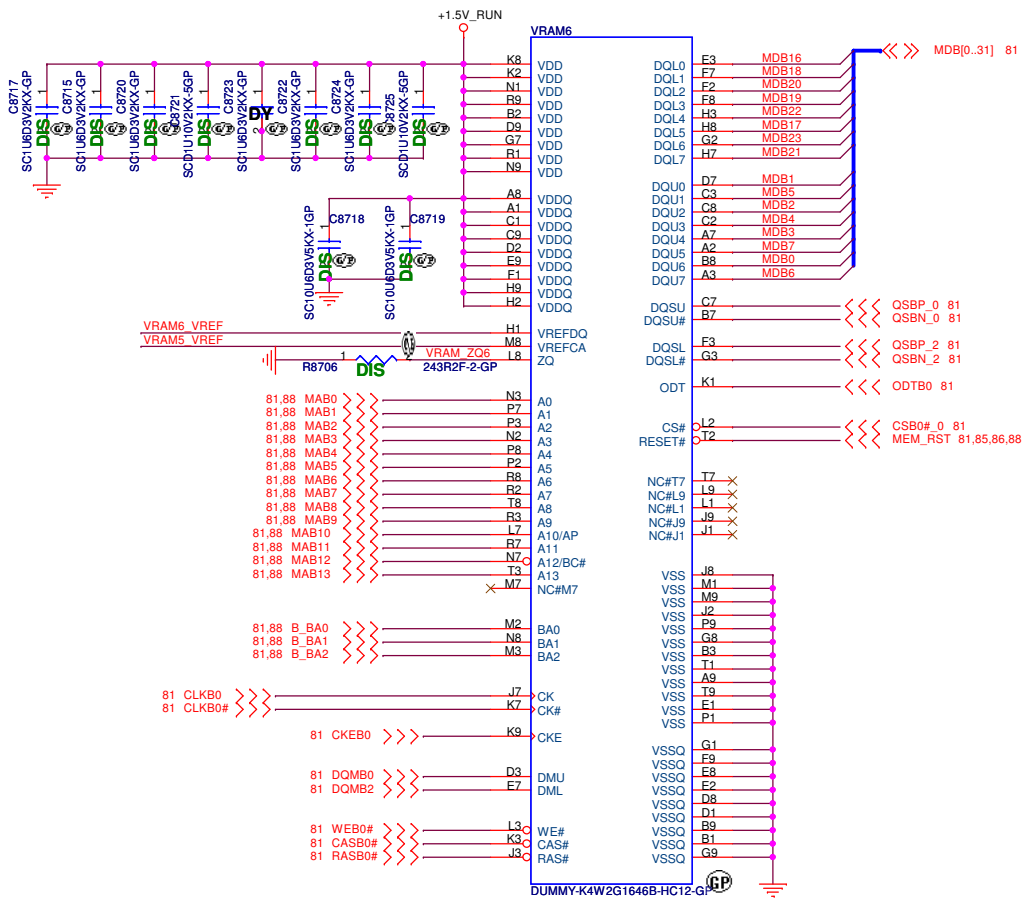
<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title <b>GPU-VRAM3,4 (2/4)</b>	
Size Custom	Document Number <b>Berry</b>	Date: Monday, July 19, 2010	Rev <b>X00</b>
Sheet 86 of 92			

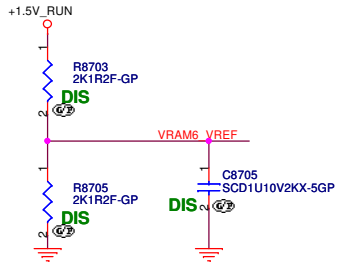
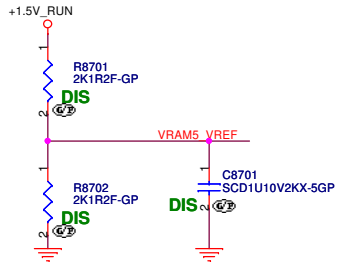


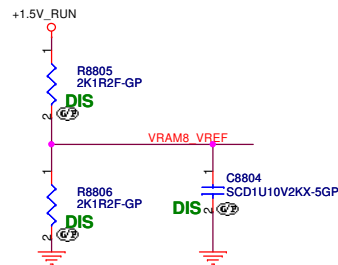
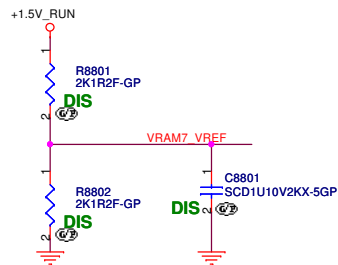
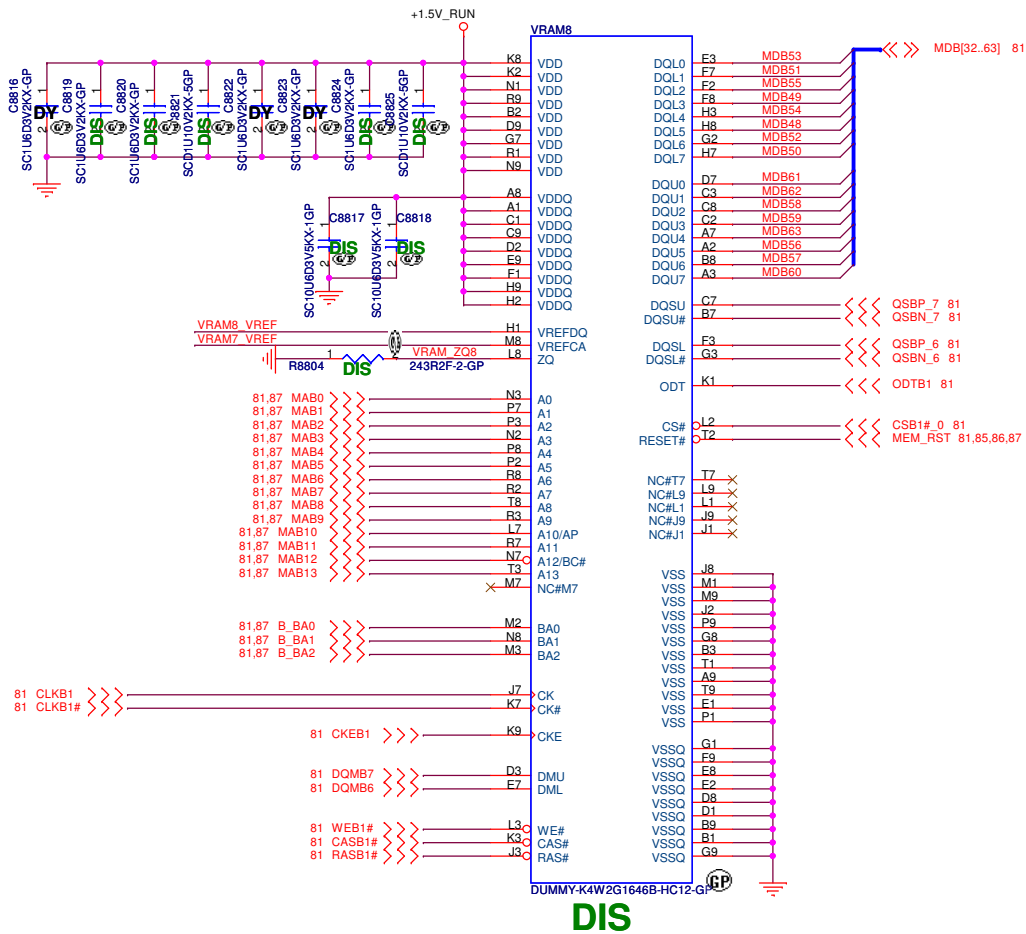
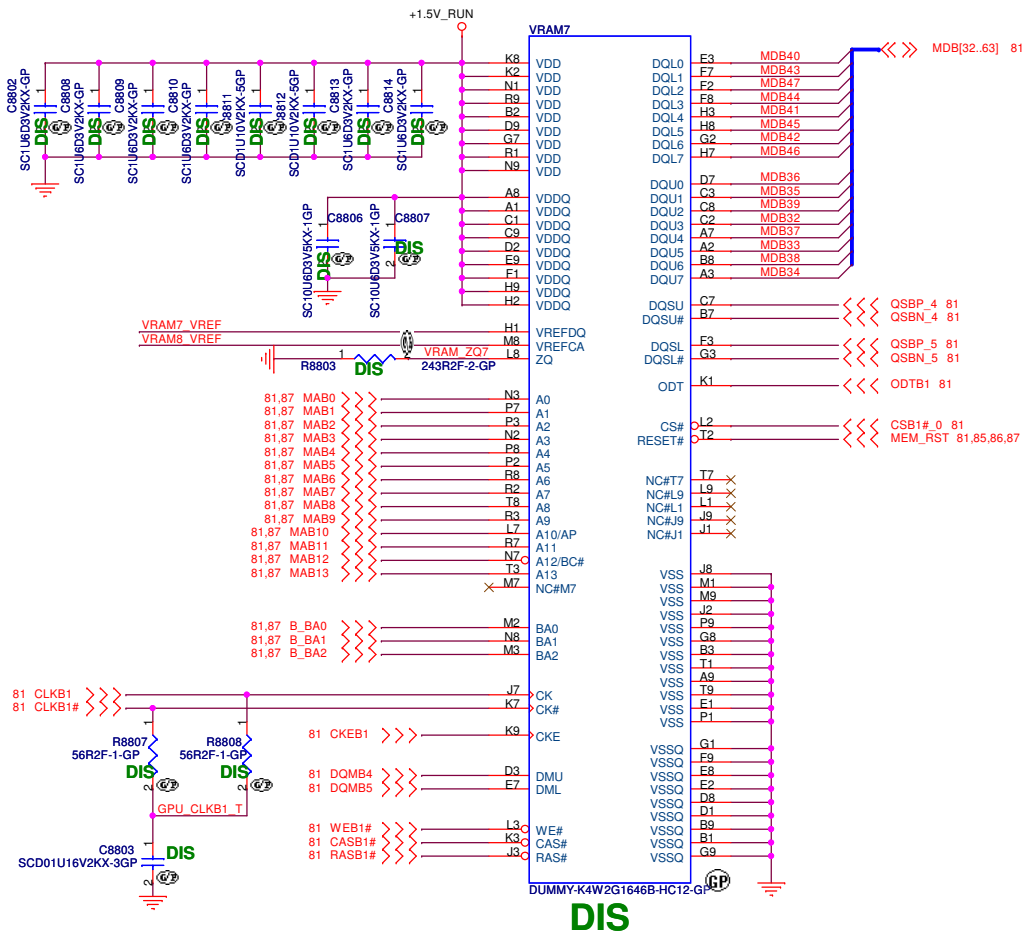


DIS



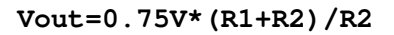
DIS







## RT8208BGQW for +VGA\_CORE



CFD\_X00\_20100513

+VGA\_CORE

Madison\_X00-20100430

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
L	L	1.12V

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
L	L	1.02V

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
L	L	1.12V

PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
L	L	1.02V

### <Core Design>

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

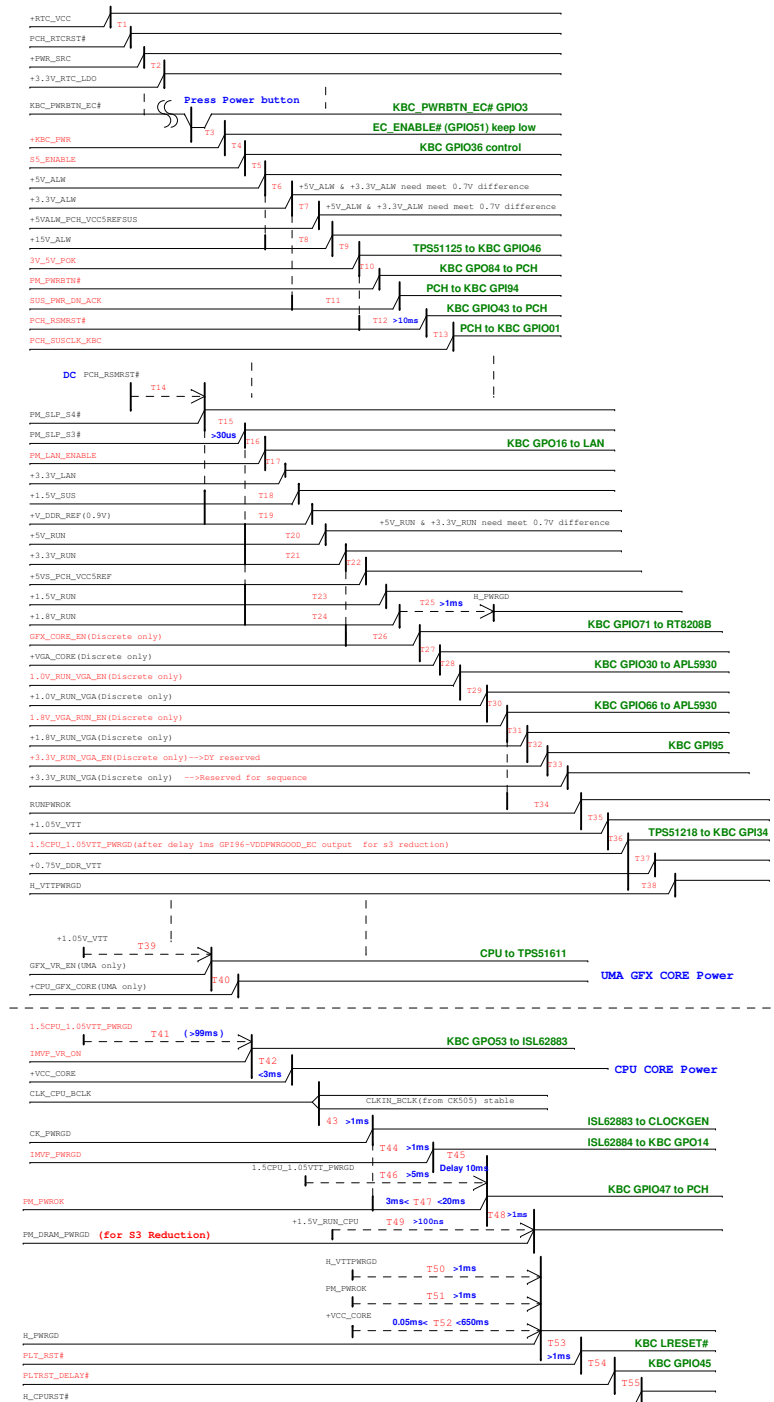
Title			
<b>RT8208B +VGA CORE</b>			
Size A3	Document Number		Rev
	<b>Arsenal DJ1 Discrete</b>		<b>X00</b>
Date:	Tuesday, July 20, 2010	Sheet 89 of 92	



(AC mode)


[illegible]

red word: KBC GPIO



(Blanking)

<Core Design>



**Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Change History**

Size	Document Number	Rev
A3	<b>Berry</b>	<b>X00</b>
Date:	Friday, May 14, 2010	Sheet 92 of 92